BAT32A239 Datasheet

Ultra-low power 32-bit microcontroller based on ARM® Cortex-M0®+

Built-in 256K bytes Flash, rich analog functions, timers and various communication interfaces

V1.0.4

Function

- **Ultra-low power operating environment:**
  - Supply voltage range: 2.0V to 5.5V
  - Temperature range: -40°C to 125°C
  - Low power modes: sleep mode, deep sleep mode
  - Operating power consumption: 120uA/MHz @64MHz
  - Power consumption in deep sleep mode: 0.8uA
  - Deep sleep mode +32.768K + RTC operation: 1.2uA
- **Kernel:**
  - ARM®32-bitCortex®-M0+ CPU
  - Operating frequency: 32KHz to 64MHz
- **Memory:**
  - 256KB Flash memory, program shared with data storage
  - 2.5KB dedicated data flash memory
  - 32KB SRAM MEMORY WITH PARITY
- **Power and reset management:**
  - Built-in power-on reset (POL) circuitry
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set).
- **Clock Management:**
  - Built-in high-speed oscillator, accuracy (±1%). A 1 MHz to 64MHz system clock and peripheral module action clock are available
  - Built-in 15KHz low-speed oscillator
  - Built-in 1 channel PLL
  - Support 1MHz ~ 20MHz external crystal oscillator, support stop vibration monitoring
  - Supports 32.768KHz external crystal oscillator for correction of internal high-speed oscillators
- **Multiplier/Divider Module:**
  - Multiplier: Supports single-cycle 32bit multiplication operations
  - Divider: Supports 32bit signed integer division and requires only 8 CPU clock cycles to complete the operation
- **Enhanced DMA controller:**
  - An interrupt triggers a start.
  - Transfer modes selectable (normal transfer mode, repeat transfer mode, block transfer mode, and chain transfer
- **Rich analog periphery:**
  - 12-bit precision ADC converter with 1.42Msps slew rate, 21 external analog channels, internal selectable PGA output as the conversion channel, temperature sensor, and support for single-channel conversion mode and multi-channel sweep conversion mode. Conversion range: 0 to positive reference voltage
  - 8-bit precision D/A converter, 2-channel analog output, real-time output function, output voltage range 0~V_{DD}
  - Comparator (CMP) with built-in two-channel hysteresis comparator, selectable input source, and selectable external reference or internal reference voltage reference
  - Programmable gain amplifier (PGA) with two channels of PGA to program 4/8/10/12/14/16/32 gains with an external GND pin that can be used as differential mode
- **Input/output port:**
  - I/O ports: 45 to 75
  - Capable of N-channel open-drain, TTL input buffering, and internal pull-up switching
  - Built-in key interrupt check-out function
  - Control circuitry with built-in clock output/buzzer output
- **Serial two-wire debugger (SWD).**
- **Rich timers:**
  - 16-bit timer: 17 channels (with PWM function and motor dedicated PWM function).
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and support for a wide range of clock correction).
  - Watchdog timer (WWDT): 1
  - SysTick timer
- **Rich and flexible interfaces:**
  - 3 serial communication unit: Serial communication unit 0 can be freely configured as 2-channel standard UART or 4-channel 3-wire SPI or 4-channel simple I^2C; Serial communication unit 1 or 2 can be freely configured as 1-channel standard UART or 2-channel 3-wire SPI or 2-channel simple I^2C; (UART of unit 0 supports LIN Bus communication, SPI00 channel supports 4-

mode)
- The source/destination field is optional for full address space range

- **Linkage Controller:**
  - It can link event signals together to achieve the linkage of peripheral functions.
  - There are 23 types of event inputs and 10 types of event triggers.

wire SPI communication)
- Standard I^2C: 2 channels
- CAN: 2 channels

- **Security features:**
  - Complies with IEC/UL 60730 related standards
  - Abnormal storage space access error is reported
  - Supports RAM parity
  - Supports hardware CRC verification
  - Supports critical SFR protection against misoperation
  - 128-bit unique ID number
  - Flash secondary protection in debug mode (level1: only flash full domain erasure, can not read and write; level2: The emulator connection is invalid and cannot be operated on flash).

- **Package:**
  - Support 48Pin, 64Pin, 80Pin multiple packages

1 Overview

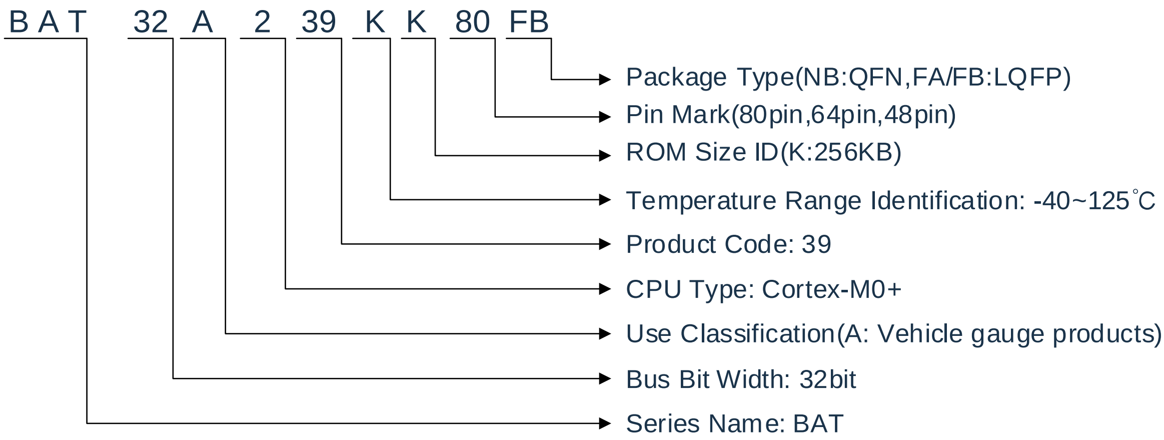
1.1 Brief Introduction

BAT32A239 series conforms to AEC-Q100 Grade1 automotive product standard, -40~125℃ operating ambient temperature, support 48~80Pin in a variety of LQFP packages. This product uses the 32bit of the high-performance ARM®Cortex-M0®+ RISC core, operating up to 64MHz, uses high-speed embedded flash memory (SRAM up to 32KB, program/data flash up to 256KB). Integrated I^2C, SPI, UART, LIN, and CAN bus and other standard interfaces. Integrated 12bit A/D converter, temperature sensor, 8bit D/A converter, comparator, programmable gain amplifier. The 12bit A/D converter can acquire external sensor signals to reduce system design costs. The 8bit D/A converter can be used for audio playback or power control. An integrated on-chip temperature sensor enables real-time monitoring of the external ambient temperature. An integrated comparator is included in the chip for applications such as control feedback from running motors or battery monitoring. Integrate a variety of advanced timer modules, load 1-channel SysTick timer, 17-channels 16 Features such as bit timer, 1-channel 15bit interval timer, watchdog timer, and real-time clock support for general-purpose PWM and motor specific PWM and other applications.

The BAT32A239 also features excellent low-power performance, supporting both sleep and deep sleep low-power modes for flexible design. It consumes 120uA/MHz @64MHz and consumes only 0.8uA in deep sleep mode for battery-powered, low-power devices. At the same time, due to the integrated event linkage controller, it can realize the direct connection between hardware modules, without CPU intervention, faster than using interrupt response, while reducing the frequency of CPU activity and prolonging battery life.

The reliability of the BAT32A239 microcontroller family, rich integrated peripheral functions, and excellent low power consumption make them suitable for a wide range of automotive product development.

1.2 List of Product Models



Product List for BAT32A239 :

Number of pins	Package	Product model
48 pins	48-pin plastic LQFP (7x7mm, 0.5mm pitch).	BAT32A239KK48FA
	48-pin plastic QFN48 (6x6mm, 0.4mm pitch).	BAT32A239KK48NB
64 pins	64-pin plastic LQFP (7x7mm, 0.4mm pitch).	BAT32A239KK64FB
80 pins	80-pin plastic LQFP (12x12mm, 0.5mm pitch).	BAT32A239KK80FA

FLASH, SRAM capacity:

Flash memory	Specific data flash memory	SRAM	BAT32A239			
			48 pins		64 pins	80 pins
256KB	2.5 KB	32KB	BAT32A239KK48FA	BAT32A239KK48NB	BAT32A239KK64FB	BAT32A239KK80FA

Product Selection Table for BAT32A239:

Part No.	Kernel	Frequency (MHz)	Minimum operating voltage (V).	Maximum operating voltage (V).	Code flash (kB)	SRAM (kB)	Data flash (kB)	DMA	GPIO	12bit ADC	8bit DAC	Comparator CMP	Amplifier PGA	Universal timer (16bit).	Real-time clock (RTC).	Watchdog timer (WDT).	Asynchronous serial bus (UART).	Synchronous serial bus (SPI).	IIC bus	LIN bus	CAN bus	Hardware multiplier	Hardware divider	Package
BAT32A239 KK48FA	M0+	64	2.0	5.5	256	32	2.5	36	45	15+4	2	2	2	17	1	1	3	5	2+5	1	1	Y	Y	LQFP 48
BAT32for239 KK48NB	M0+	64	2.0	5.5	256	32	2.5	36	45	15+4	2	2	2	17	1	1	3	5	2+5	1	1	Y	Y	QFN 48
BAT32A239 KK64FB	M0+	64	2.0	5.5	256	32	2.5	37	59	16+4	2	2	2	17	1	1	3	6	2+6	1	1	Y	Y	LQFP 64
BAT32A239 KK80FA	M0+	64	2.0	5.5	256	32	2.5	37	75	21+4	2	2	2	17	1	1	4	8	2+8	1	2	Y	Y	LQFP 80

1.3 Top View

1.3.1 BAT32A239KK48FA

- 48-pin plastic LQFP (7x7mm, 0.5mm pitch).

Note: The functions in ( ) of above Figure can be assigned by setting the peripheral I/O redirection registers.

1.3.2 BAT32A239KK48NB

• 48-pin plastic QFN48 (6x6mm, 0.4mm pitch).

Note: The functions in ( ) of above Figure can be assigned by setting the peripheral I/O redirection registers.

1.3.3 BAT32A239KK64FB

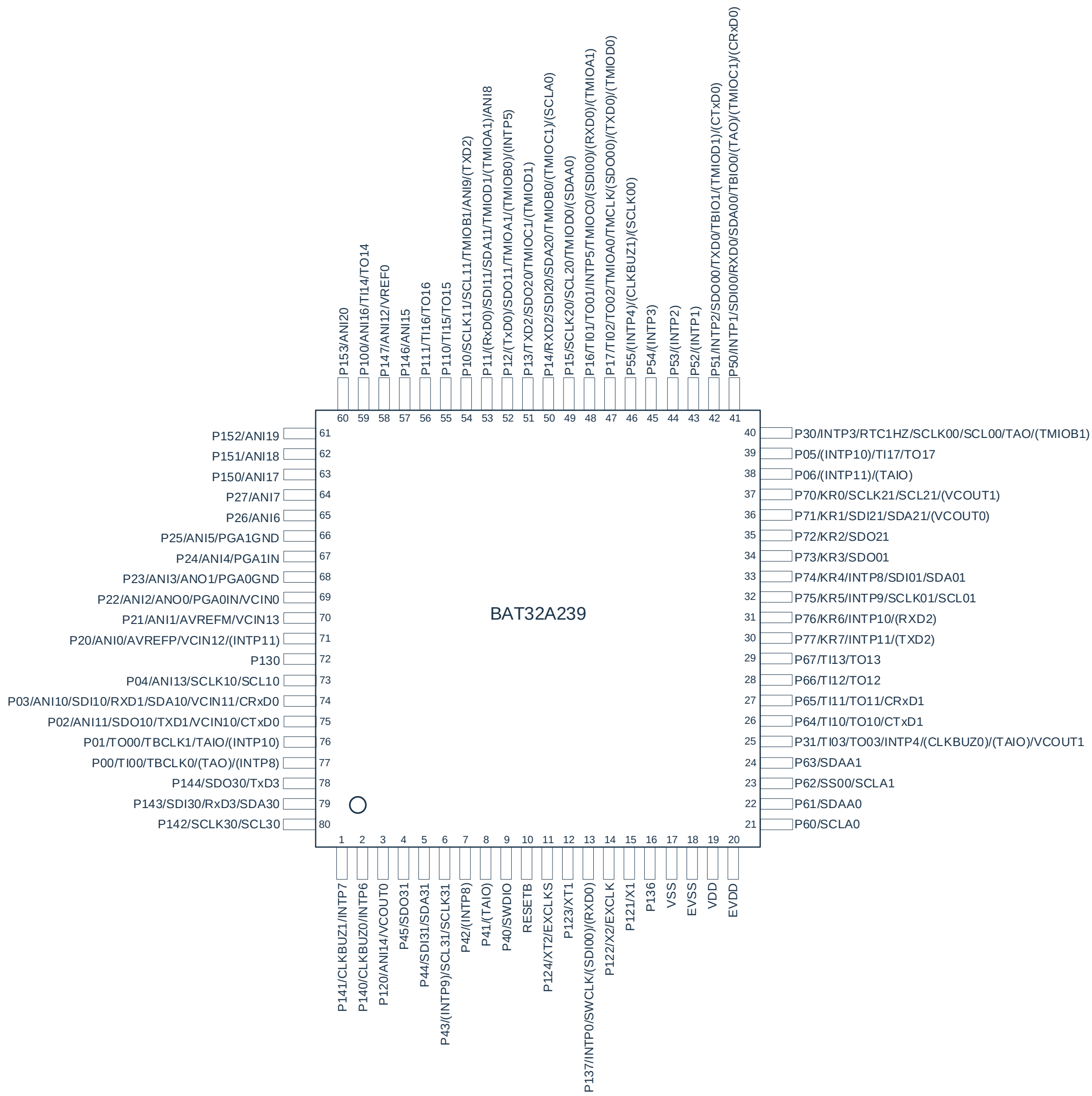
- 64-pin plastic LQFP (7x7mm, 0.4mm pitch).

Note:

1. The EV_{SS} pin and the V_{SS} pin must be in the same potential.
2. The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.
3. In the case of application areas where it is necessary to reduce the noise generated from the inside of the microcontroller, noise countermeasures such as providing separate power to V_{DD} and EV_{DD} and grounding V_{SS} and EV_{SS} separately are recommended.
4. The functions in the preceding figure ( ) can be assigned by setting the peripheral I/O redirection registers.

1.3.4 BAT32A239KK80FA

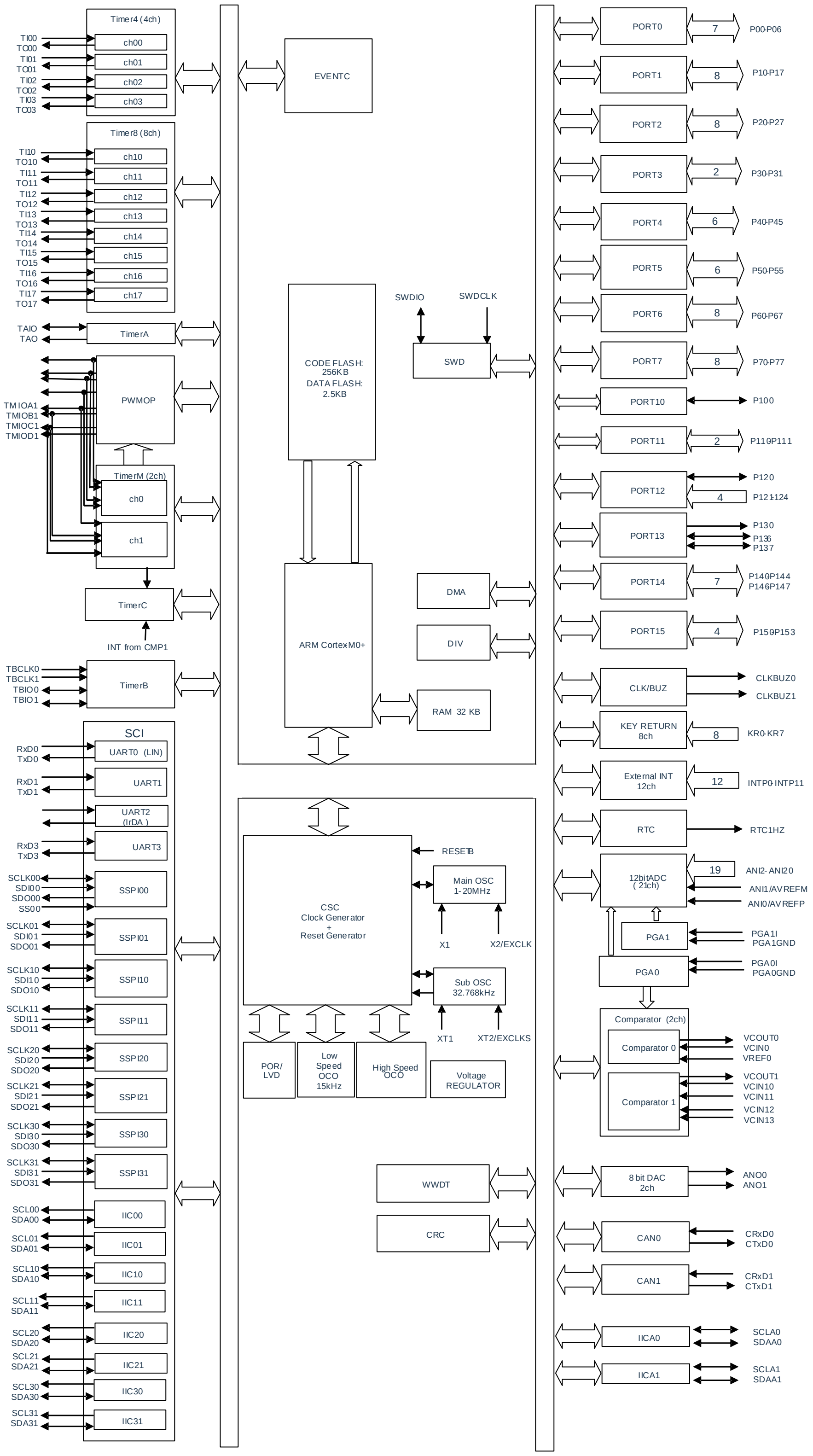
- 80-pin plastic LQFP (12x12mm, 0.5mm pitch).



Note:

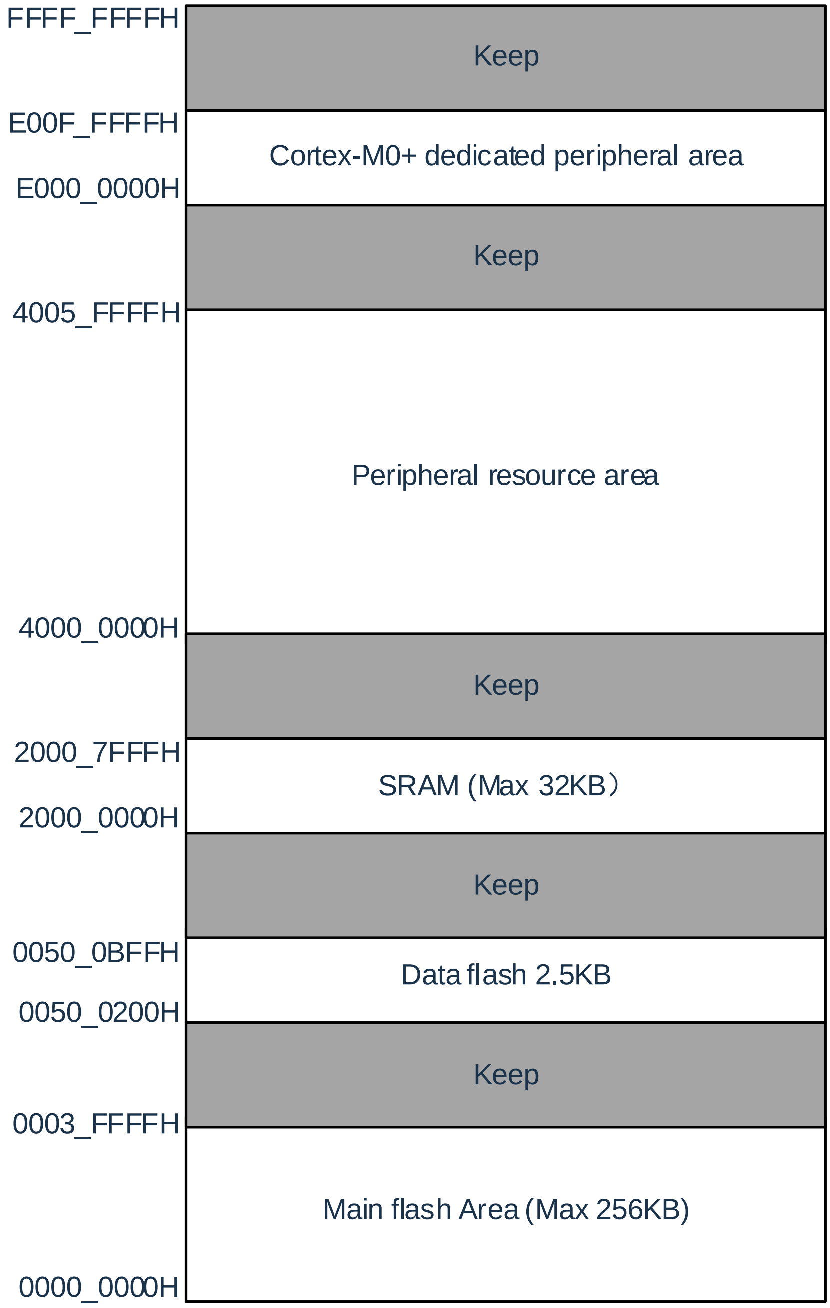
1. The EV_{SS} pin and the V_{SS} pin must be in the same potential.
2. The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.
3. In the case of application areas where it is necessary to reduce the noise generated from the inside of the microcontroller, noise countermeasures such as providing separate power to V_{DD} and EV_{DD} and grounding V_{SS} and EV_{SS} separately are recommended.
4. The functions in the preceding figure ( ) can be assigned by setting the peripheral I/O redirection registers.

2 Product Structure Diagram



Note: The above figure is a block diagram of an 80-pin product, and some functions of products below 80 pin are not supported.

3 Memory Mapping



4 Pin Function

4.1 Port Functionality

The relationship between the power supply and the pin is shown below

80-pin, 64-pin product:

Power/Ground	The Corresponding Pin
EV_{DD}/EV_{SS}	• Port pins other than P20~P27, P121~P124, P137 and RESETB
V_{DD}/V_{SS}	• P20~P27, P121~P124, P137 and RESETB

The 48-pin product uses a single power supply, and all pins are powered by V_{DD}.

All ports of this product are divided into five types by type, which are type1 to type5, and the corresponding conditions are as follows:

Type 1: Bidirectional I/O function

Type 2: NOD function, corresponding to pin P60-P63

Type 3: Only input functions, such as clocks, correspond to pins P121-P124

Type 4: Output function only, corresponding to pin P130

Type 5: RESET function, corresponding to pin RESETB

For details of the lead frame diagrams for each type, see 4.3 Port types

4.1.1 48 Pin Product Pin Function Description

(1/2)

The feature name	Port type	Input / output	After the reset is released	Multiplexing function	Function
P00	Type 1	Input / output	Analog function	ANI11/TXD1/VCIN10/TI00/TBCLK0/(TAO) /(INTP8)/CTxD0	Port 0 2-bit input/output port, which can be specified as input or output in bits. The input port can be set by software using an internal pull-up resistor. The input of P01 can be set to TTL input buffering. The output of P00 can be set to an N-channel open-drain output (V_{DD} withstand voltage). P00 and P01 can be set to analog inputs.
P01				ANI10/RXD1/VCIN11/TO00/TBCLK1 /TAIO/INTP10/CRxD0	
P10		Input / output	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1 An 8-bit input /output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor The inputs for P10 and P14~ P17 can be set to TTL Input buffering. The outputs of P10, P11, P13~P15, and P17 can be programmed to N-channel open-drain outputs (V_{DD} Withstand pressure). P10 and P11 can be set to analog inputs.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)	
P13				TxD2/SDO20/TMIOC1/(TMIOD1)	
P14				RxD2/SDI20/SDA20/ TMIOB0/(TMIOC1)/ (SCLA0)	
P15				SCLK20/SCL20/TMIOD0/(SDAA0)/CLKB UZ1	
P16				TI01/TO01/INTP5/TMIOC0/(RXD0)/(TMIOA1)	
P17				TI02/TO02/TMIOA0/TMCLK/(TXD0) /(TMIOD0)	
P20		Input / output	Analog function	ANI0/AVREFP/VCIN12/INTP11	Port 2 An 8-bit input /output port that can be specified as an input or output in bits. Can be set to analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P30		Input / output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3 2-bit input/output port, can be specified as input or output in bits. The input port can be set by software using an internal pull-up resistor
P31				TI03/TO03/INTP4/(CLKBUZ0)/(TAIO) /VCOUT1	

					The input of the P30 can be set to TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (V_{DD} withstand voltage).
P40		Input / output	Input port	SWDIO	Port 4
P41				(TAIO)	2-bit input/output port, can be specified as input or output in bits. The input port can be set by software using an internal pull-up resistor.

(2/2)

Function name	Port type	Input / output	After the reset is released	Multiplexing function	Function
P50	Type 1	Input / output	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5 2-bit input/output port, which can be specified as input or output in bits. The input port can be set by software using an internal pull-up resistor. The input of the P50 can be set to TTL input buffering. The outputs of P50 and P51 can be set to N-channel open-drain outputs (V_{DD} withstand voltage).
P51				INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P60	Type 2	Input / output	Input port	SCLA0	Port 6 A 4-bit input /output port that can be specified as an input or output in bits. The output of P60 to P63 is an N-channel open-drain output (6V withstand voltage).
P61				SDAA0	
P62				SS00	
P63				—	
P70	Type 1	Input / output	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7 A 6-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The outputs of P71 and P74 can be programmed to N-channel open-drain outputs (V_{DD} withstand voltage).
P71				KR1/SDI21/SDA21/(VCOUT0)	
P72				KR2/SDO21/(TXD1)	
P73				KR3/SDO01/(RXD1)	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P120		Input / output	Analog function	ANI14/VCOUT0	Port 12 1-bit input /output port and 4-bit input dedicated port. Only the P120 has an output function. Only the input port of the P120 can be set by software to use the internal pull-up resistor. The P120 can be set to an analog input.
P121	Type 3	input	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P130	Type 4	output	Output port	—	Port 13 1-bit output dedicated ports and 2-bit input/output ports, P136 and P137 can be specified as inputs or outputs in bits. The input port can be set by software using internal pull-up resistors.
P136	Type 1	Input/ output	Input port	INTP0	
P137				SWCLK	
P140		Input/ output	Input port	CLKBUZ0/INTP6	Port 14 A 3-bit input /output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. P146, P147 can be set to analog input.
P146			Analog function	ANI15	
P147				ANI12/VREF0	
RESETB	Type 5	input	—	—	Input-specific pin for external reset When no external reset is used, it must be connected to the V_{DD} directly or via a resistor.

Note:

1. Set each pin to digital or analog (can be set in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in Table ( ) above can be assigned by setting the peripheral I/O redirection registers.

4.1.2 64 Pin Product Pin Function Description

(1/2)

Function name	Port type	Input / output	After the reset is released	Multiplexing function	Description of the feature
P00	Type 1	Input / output	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0 A 7-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs for P01, P03, and P04 can be set to TTL Input buffering. The outputs of P00 and P02~ P04 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P02, P03, P04 can be set as analog inputs.
P01				TO00/TBCLK1/TAIO/(INTP10)	
P02			Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03				ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04				ANI13/SCLK10/SCL10	
P05			Input port	(INTP10)	
P06				(INTP11)/(TAIO)	
P10		Input / output	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs for P10 and P14~ P17 can be set to TTL Input buffering. The outputs of P10, P11, P13~P15, and P17 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P10 and P11 can be set to analog inputs.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13				TXD2/SDO20/TMIOC1/(TMIOD1)	
P14				RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15				SCLK20/SCL20/TMIOD0/ (SDAA0)	
P16				TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0)/(TMIOA1)	
P17				TI02/TO02/TMIOA0/TMCLK/(SDO00)/(TXD0)/(TMIOD0)	
P20		Input / output	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2 An 8-bit input/output port that can be specified as an input or output in bits. Can be set to analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P30		Input / output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/(TMIOB1)	Port 3 2-bit input/output port, which can be specified as input or output in bits. The input port can be set by software using
P31				TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	

					an internal pull-up resistor. The input of the P30 can be set to TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (EV_{DD} withstand voltage).

(2/2)

Function name	Port type	Input / output	After the reset is released	Multiplexing function	Function
P40	Type 1	Input / output	Input port	SWDIO	Port 4 A 4-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor.
P41				(TAIO)	
P42				(INTP8)	
P43				(INTP9)	
P50		Input / output	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/ (TAO) /(TMIOC1)/(CRxD0)	Port 5 A 6-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs of P50 and P55 can be set to TTL input buffers. The outputs of the P50, P51, and P55 can be set to N-channel open-drain output (EV_{DD} withstand voltage).
P51				INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52				(INTP1)	
P53				(INTP2)	
P54				(INTP3)	
P55				(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	Type 2	Input / output	Input port	SCLA0	Port 6 A 4-bit input/output port that can be specified as an input or output in bits. The output of P60 to P63 is an N-channel open-drain output (6V withstand voltage).
P61				SDAA0	
P62				SS00/SCLA1	
P63				SDAA1	
P70	Type 1	Input / output	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The outputs of the P71 and P74 can be set to N-channel open-drain output (EV_{DD} withstand voltage).
P71				KR1/SDI21/SDA21/(VCOUT0)	
P72				KR2/SDO21	
P73				KR3/SDO01	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P76				KR6/INTP10/(RxD2)	
P77				KR7/INTP11/(TxD2)	
P120		Input / output	Analog function	ANI14/VCOUT0	Port 12 1-bit input /output port and 4-bit input dedicated port Only P120 can specify inputs or outputs. Only the input port of the P120 can be set
P121	Type 3	input	Input port	X1	
P122				X2/EXCLK	
P123				XT1	

<table>
<tr><td>P124</td><td></td><td></td><td></td><td>XT2/EXCLKS</td><td>by software to use the internal pull-up resistor. The P120 can be set to an analog input.</td></tr>
<tr><td>P130</td><td>Type 4</td><td>output</td><td>Output port</td><td>—</td><td rowspan="3">Port 13
1-bit output dedicated port and 2-bit input/output port, P136 and P137 can be specified as input or output in bits. The input port can be set by software using internal pull-up resistors.</td></tr>
<tr><td>P136</td><td rowspan="7">Type 1</td><td rowspan="2">Input/ output</td><td rowspan="2">Input port</td><td>INTP0</td></tr>
<tr><td>P137</td><td>SWCLK</td></tr>
<tr><td>P140</td><td rowspan="4">Input / output</td><td rowspan="2">Input port</td><td>CLKBUZ0/INTP6</td><td rowspan="4">Port 14
4-bit input/output port, can be specified as input or output in bits. The input port can be set by software using an internal pull-up resistor.
P146, P147 can be set to analog input.</td></tr>
<tr><td>P141</td><td>CLKBUZ1/INTP7</td></tr>
<tr><td>P146</td><td rowspan="2">Analog function</td><td>ANI15</td></tr>
<tr><td>P147</td><td>ANI12/VREF0</td></tr>
<tr><td>RESETB</td><td>Type 5</td><td>input</td><td>—</td><td>—</td><td>An input pin dedicated to an external reset must be connected to V_{DD} directly or via a resistor when no external reset is used.</td></tr>
</table>

Note:

1. Set each pin to digital or analog (can be set in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in Table ( ) above can be assigned by setting the peripheral I/O redirection registers.

4.1.3 80 Pin Product Pin Function Description

(1/2)

Function name	Port type	Input / output	After the reset is released	Multiplexing function	Description of the feature
P00	Type 1	Input / output	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0 A 7-bit input /output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs for P01, P03, and P04 can be set to TTL Input buffering. The outputs of P00 and P02~ P04 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P02, P03, P04 can be set as analog inputs.
P01				TO00/TBCLK1/TAIO/(INTP10)	
P02			Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03				ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04				ANI13/SCLK10/SCL10	
P05			Input port	(INTP10)/TI17/TO17	
P06				(INTP11)/(TAIO)	
P10		Input / output	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1 An 8-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs for P10 and P14~ P17 can be set to TTL Input buffering. The outputs of P10, P11, P13~P15, and P17 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P10 and P11 can be set to analog inputs.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13				TXD2/SDO20/TMIOC1/(TMIOD1)	
P14				RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)	
P15				SCLK20/SCL20/TMIOD0/(SDAA0)	
P16				TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0) /(TMIOA1)	
P17				TI02/TO02/TMIOA0/TMCLK/(SDO00) /(TXD0)/(TMIOD0)	
P20		Input / output	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2 An 8-bit input /output port that can be specified as an input or output in bits. Can be set to analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P30		Input / output	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO /(TMIOB1)	Port 3 2-bit input/output port, which can be specified as input or output in bits. The
P31				TI03/TO03/INTP4/(CLKBUZ0)/(TAIO	

				) /VCOUT1	input port can be set by software using an internal pull-up resistor. The input of the P30 can be set to TTL input buffering. The output of the P30 can be set to an N-channel open-drain output (EV_{DD} withstand voltage).

(2/2)

Function name	Port type	Input / output	After the reset is released	Multiplexing function	Function
P40	Type 1	Input / output	Input port	SWDIO	Port 4 A 6-bit input /output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs of P43 and P44 can be set to TTL input buffers and the outputs to N-channel open-drain outputs (EV_{DD} withstand voltage).
P41				(TAIO)	
P42				(INTP8)	
P43				(INTP9)/SCLK31/SCL31	
P44				SDA31/SDI31	
P45				SDO31	
P50		Input / output	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5 A 6-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs of P50 and P55 can be set to TTL input buffers. The outputs of the P50, P51, and P55 can be set to N-channel open-drain output (EV_{DD} withstand voltage).
P51				INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52				(INTP1)	
P53				(INTP2)	
P54				(INTP3)	
P55				(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	Type 2	Input / output	Input port	SCLA0	Port 6 An 8-bit input/output port that can be specified as an input or output in bits. The output of P60 to P63 is an N-channel open-drain output (6V withstand voltage).
P61				SDAA0	
P62				SS00/SCLA1	
P63				SDAA1	
P64	Type 1			TI10/TO10/CTxD1	
P65				TI11/TO11/CRxD1	
P66				TI12/TO12	
P67				TI13/TO13	
P70		Input / output	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7 An 8-bit input /output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The outputs of the P71 and P74 can be
P71				KR1/SDI21/SDA21/(VCOUT0)	
P72				KR2/SDO21	
P73				KR3/SDO01	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	

P76				KR6/INTP10/(RxD2)	set to N-channel open-drain output (EV_{DD} withstand voltage).
P77				KR7/INTP11/(TxD2)	
P100		Input / output	Analog function	ANI16/TI14/TO14	Port 10 A 1-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor.
P110		Input / output	Input port	TI15/TO15	Port 11 2-bit input/output port, which can be specified as input or output in bits. The input port can be set by software using an internal pull-up resistor.
P111				TI16/TO16	
P120	Type 1	Input / output	Analog function	ANI14/VCOUT0	Port 12 1-bit input /output port and 4-bit input dedicated port Only P120 can specify inputs or outputs. Only the input port of the P120 can be set by software to use the internal pull-up resistor. The P120 can be set to an analog input.
P121	Type 3	input	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P130	Type 4	output	Output port	—	Port 13 1-bit output dedicated port and 2-bit input/output port, P136 and P137 can be specified as input or output in bits. The input port can be set by software using internal pull-up resistors.
P136	Type 1	Input/ output	Input port	—	
P137				/INTP0/SWCLK/(SDI00)/(RXD0)	
P140		Input / output	Input port	CLKBUZ0/INTP6	Port 14 A 7-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. The inputs of the P142 and P143 can be set to TTL input buffering. The output of the P142, P143, P144 can be set to N-channel open-drain output (EV_{DD} withstand voltage). P146, P147 can be set to analog input.
P141				CLKBUZ1/INTP7	
P142				SCLK30/SCL30	
P143				SDI30/RxD3/SDA30	
P144				SDO30/TxD3	
P146			Analog function	ANI15	
P147				ANI12/VREF0	
P150		Input / output	Analog function	ANI17	Port 15 A 4-bit input/output port that can be specified as an input or output in bits. The input port can be set by software using an internal pull-up resistor. Can be set to analog input.
P151				ANI18	
P152				ANI19	
P153				ANI20	
RESETB	Type 5	input	—	—	An input pin dedicated to an external

					reset must be connected to V_{DD} directly or via a resistor when no external reset is used.

Note:

1. Set each pin to digital or analog (can be set in bits) via port mode control register x (PMCx).
2. For a description of the multiplexing function, see "4.2 Port Multiplexing Function".
3. The functions in Table ( ) above can be assigned by setting the peripheral I/O redirection registers.

4.2 Port Multiplexing Function

(1/2)

The feature name	Input/output	Function
ANI0 ~ ANI20	Input	The analog input of the A/D converter
ANO0, ANO1	output	The output of the D/A converter
INTP0 ~ INTP11	Input	External interrupt request input Designation of effective edges: ascending edges, falling
VCIN0	Input	The analog voltage input for comparator 0
VCIN10, VCIN11, VCIN12, VCIN13	Input	The analog voltage/reference input for comparator 1
VREF0	Input	The reference input for comparator 0
VCOUT0, VCOUT1	output	Comparator output
PGA0IN, PGA1IN	Input	PGA input
PGA0GND, PGA1GND	Input	PGA reference input
KR0 ~ KR7	Input	The key interrupts the input
CLKBUZ0, CLKBUZ1	output	Clock output / buzzer output
RTC1HZ	output	Correction clock (1Hz) output for the real-time clock
RESETB	Input	A active-low system reset input must be connected to V_{DD} directly or via a resistor when no external reset is used.
CRxD0, CRxD1	Input	Serial data input for CAN
CTxD0, CTxD1	output	Serial data output for CAN
RxD0 ~ RxD3	Input	Serial interface UART0, UART1, UART2 serial data input
TxD0 ~ TxD3	output	Serial interface UART0, UART1, UART2 serial data output
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCL30, SCL31	output	Serial clock output for the serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31	Input / output	Serial data input/output for serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21, IIC30, IIC31
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21, SCLK30, SCLK31	Input / output	Serial interface serial clock input/output for SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21, SDI30, SDI31	Input	Serial data input for serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31

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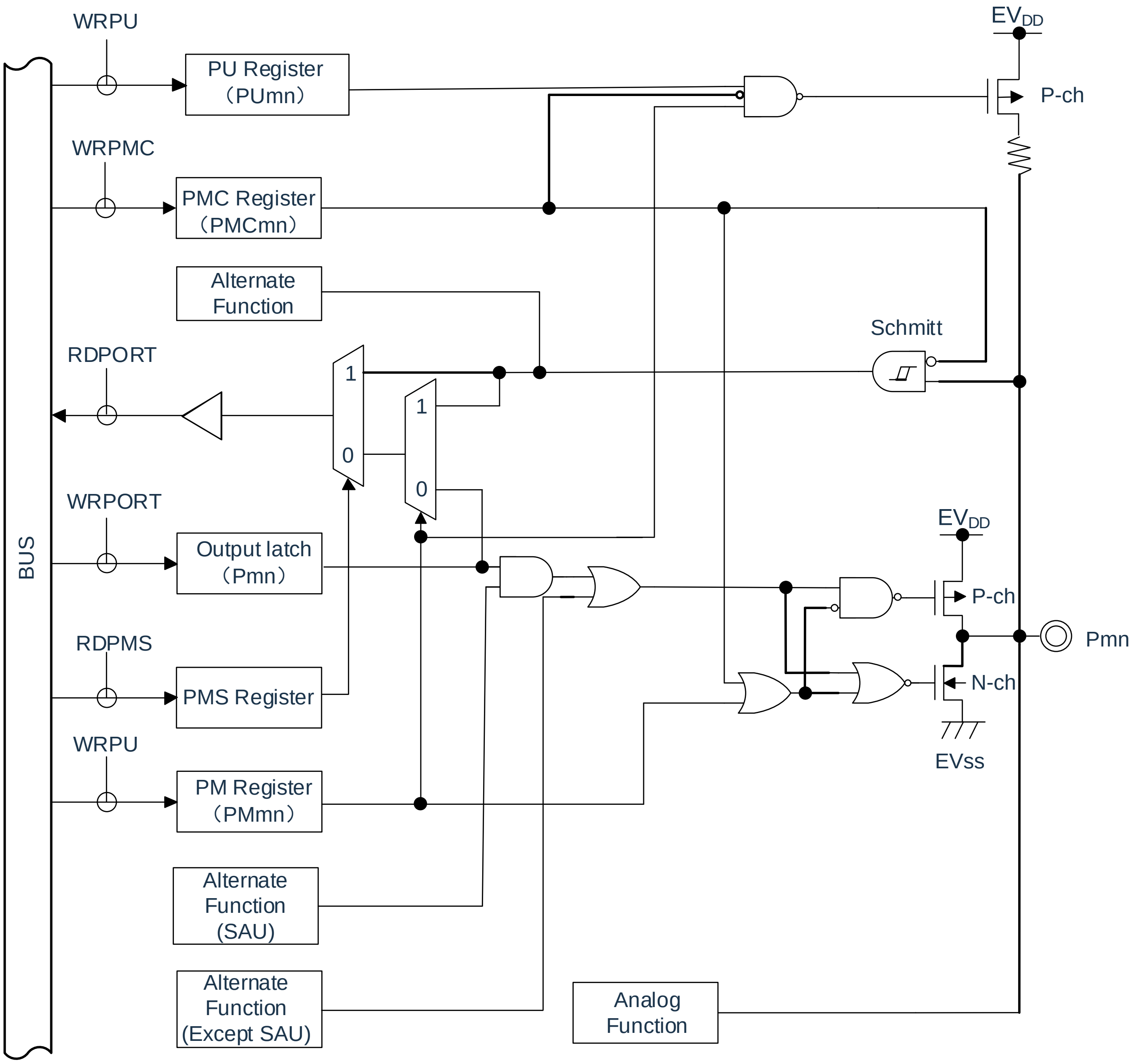
The feature name	Input/output	Function
SS00	Input	Chip select input for serial interface SSPI00
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21, SDO30, SDO31	output	Serial data output for SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21, SSPI30, SSPI31
SCLA0, SCLA1	Input/output	Serial interface IICA0, IICA1 clock input/output
SDAA0, SDAA1	Input/output	Serial interface IICA0, IICA1 serial data input/output
TUE00 ~ TI03	Input	External counting clock/capture trigger input for 16-bit timer Timer4
TO00 ~ TO03	output	Timer output of the 16-bit timer Timer4
TI10 ~ TI17	Input	External count clock/capture trigger input for 16-bit timer Timer8
TO10 ~ TO17	output	Timer output of the 16-bit timer Timer8
TAIO	Input/output	The input/output of timer TimerA
MAN	output	The output of timer TimerA
TMCLK	Input	Timer TimerM for the external clock input
TMIOA0, TMIOB0, TMIOC0,	Input/output	Timer TimerM input/output
TBIO0, TBIO1	Input/output	The input/output of timer TimerB
TBCLK0, TBCLK1	Input	The external clock input for timer TimerB
X1, X2	—	Connect the resonator used for the master system clock.
EXCLK	Input	The external clock input to the master system clock
XT1, XT2	—	Connect a resonator for the subsystem clock.
EXCLKS	Input	An external clock input to the secondary system clock
V_{DD}	—	＜48Pin product＞:Power supply for all pins ＜64,80Pin product＞: Power supplies for P20 to P27, P121 to P124, P137, and RESETB pins
EV_{DD}	—	Power supplies for port pins (except P20 to P27, P121 to P124, P137, and RESETB).
AV_{REFP}	Input	The positive (+) reference input of the A/D converter
AV_{REFM}	Input	The negative (-) reference voltage input for the A/D converter
V_{SS}	—	＜48Pin product＞:Ground potential of all pins ＜64,80Pin product＞: Ground potentials of the P20 to P27, P121 to P124, P137 and RESETB .
EV_{SS}	—	The ground potential of the port pins (except P20 to P27, P121 to P124, P137, and RESETB).
SWDIO	Input/output	SWD data interface
SWCLK	Input	SWD clock interface

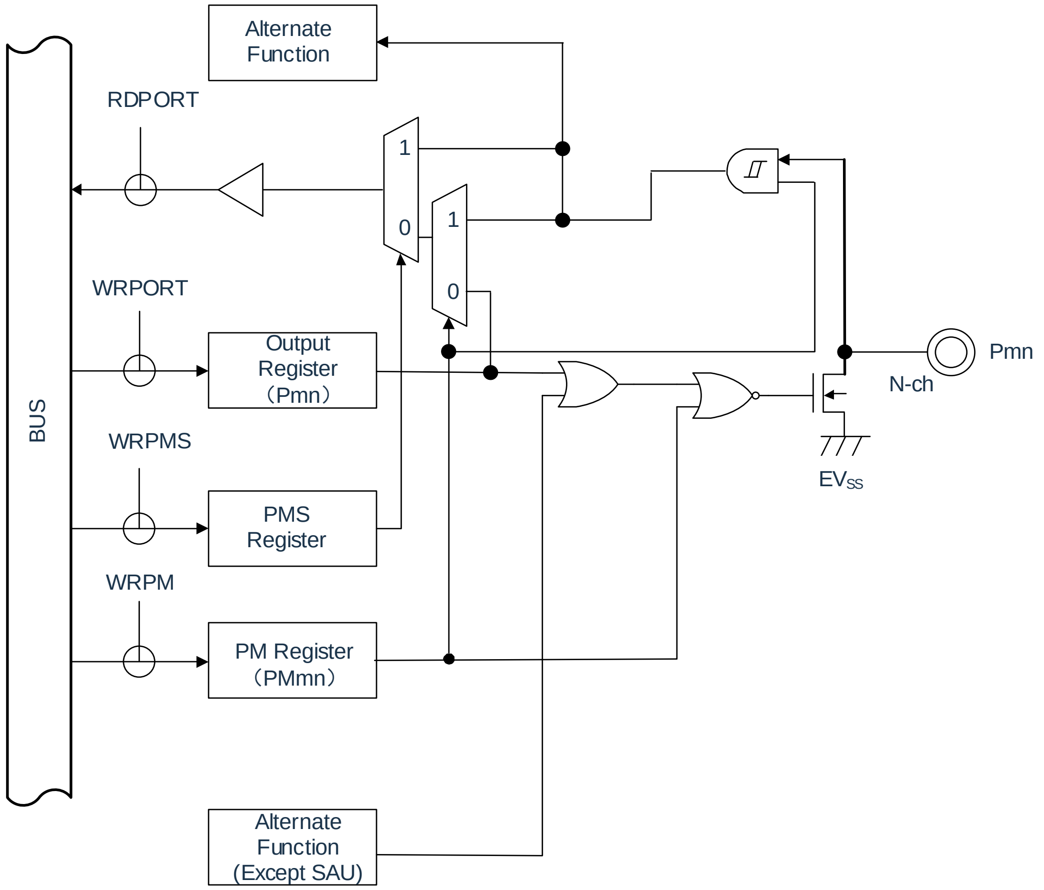
Note: As a countermeasure to noise and lockout, the bypass capacitor (around 0.1uF) must be connected at the shortest distance between V_{DD}-V_{SS} and EV_{DD}-EV_{SS} and with thicker wiring.

4.3 The Port Type

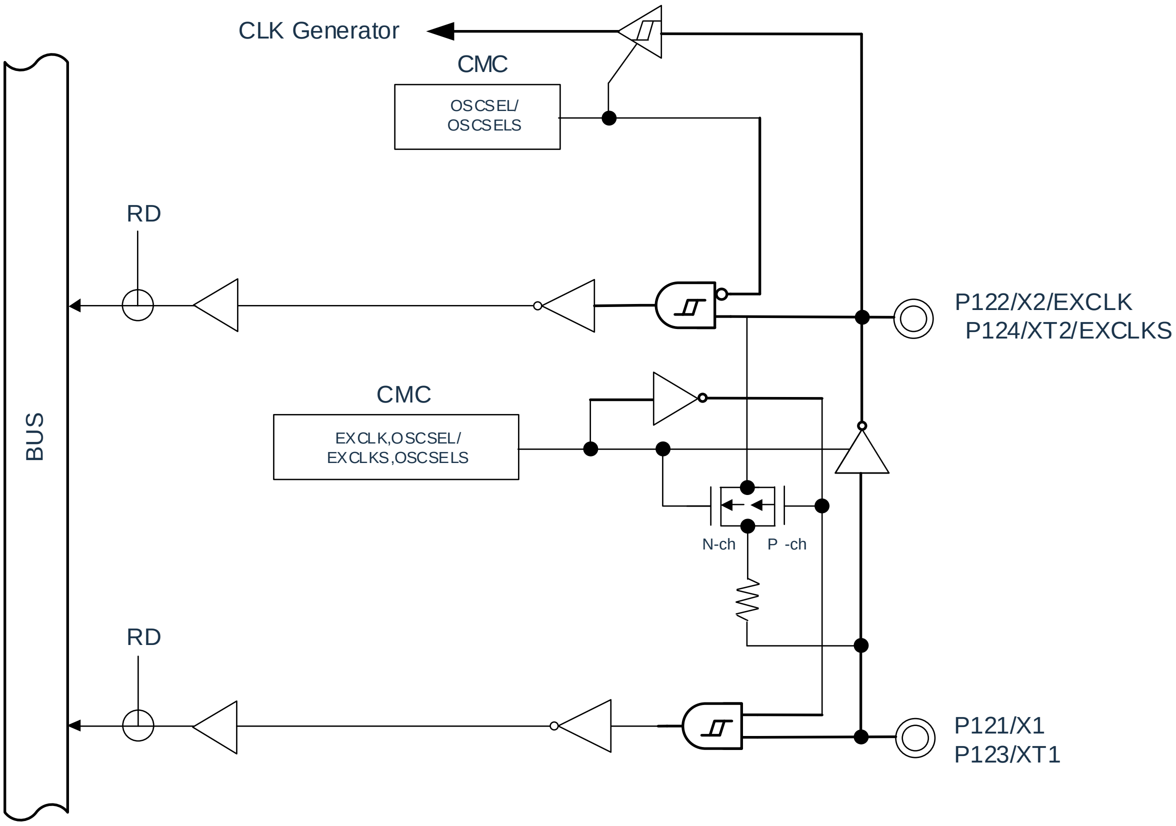
Type 1: Bidirectional I/O capability



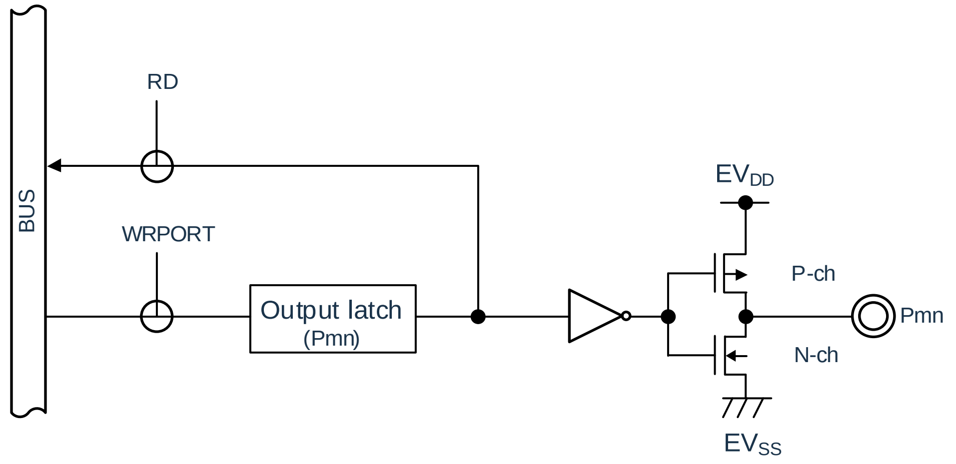
Type 2: NOD functionality



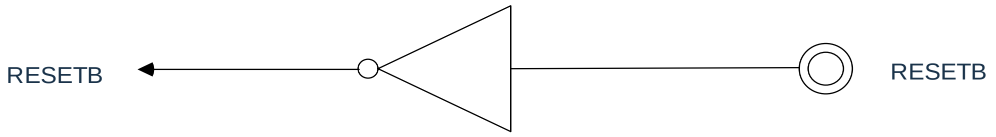
Type 3: Input function only



Type 4: Output function only



Type 5: RESET function



5 Feature Overview

5.1 ARM® Cortex-M0®+ Core

ARM's Cortex-M0+ processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of low pin count and low power microcontrollers while providing excellent computing performance and advanced system response to interrupts.

The Cortex-M0+ processor's 32-bit RISC processor provides superior code efficiency and provides the high performance expectations of the ARM core, unlike 8-bit and 16-bit devices of the same memory size. The Cortex-M0+ processor has 32 address lines and up to 4G of storage.

The Cortex-M0+ processor in this product integrates the MPU memory protection unit: providing a hardware way to manage and protect memory and control access rights.

The BAT32A239 uses an embedded ARM core and is therefore compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash Memory

The BAT32A239 has built-in flash memory that can be programmed, erased, and rewritten. It has the following functions:

- Programs and data share 256K of storage.
- 2.5KB dedicated data flash memory
- Support page erase, each page size is 512byte
- Support byte/half-word/word (32bit) programming

5.2.2 SRAM

The BAT32A239 has a built-in 32K byte embedded SRAM.

5.3 Enhanced DMA Controller

The built-in enhanced DMA (Direct Memory Access) controller enables data transfer between memories without using a CPU.

- Supports start-up DMA via peripheral interrupts, enabling real-time control via communication, timers, and A/D.
- The source/destination field is optional for the full address space range (when the flash field is the destination address, flash needs to be preset as the programming mode).
- Supports 4 transfer modes (normal transfer mode, repeat transfer mode, block transfer mode, and chain transfer mode).

5.4 Linkage Controller

The linkage controller links the events output by each peripheral function with the peripheral function trigger source. This enables collaborative operation between peripheral functions without using the CPU.

The UMC has the following functions:

- It can link event signals together to achieve the linkage of peripheral functions.
- There are 23 types of event inputs and 10 kinds of event triggers.

5.5 The Clock Generation and Start Up

A clock generation circuit is a circuit that generates a clock to the CPU and peripheral hardware. There are three types of system clock and clock oscillation circuitry.

5.5.1 The Master System Clock

- X1 oscillation circuit: It can generate a clock oscillation of 1 to 20MHz by connecting a resonator to the pins (X1 and X2), and can stop the oscillation by executing a deep sleep command or setting MSTOP.
- High Speed Internal Oscillator (High Speed OCO): Oscillates by selecting the frequency via option bytes. After the reset is released, the CPU starts operation by default with this high-speed internal oscillator clock. Oscillation can be stopped by executing a deep sleep command or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The maximum frequency is 64Mhz and the accuracy is ± 1.0%.
- Input to the external clock by pin (X2): (1~20MHz) and can be invalidated by executing a deep sleep instruction or setting the MSTOP bit.

5.5.2 Auxiliary System Clock

- XT1 oscillation circuit: Generates a clock oscillation of 32.768kHz by connecting a 32.768kHz resonator to pins (XT1 and XT2) and can be set to XTSTOP The bit stops the oscillation.
- Input external clock by pin (XT2): 32.768kHz, and can set the input of the external clock to be invalid by setting the XTSTOP bit.

5.5.3 Low-speed Internal Oscillator Clock

- Low-speed internal oscillator (low-speed OCO): Produces 15kHz (typical) The clock oscillates. You cannot use a low-speed internal oscillator clock as a CPU clock. Only the following peripheral hardware can operate through a low-speed internal oscillator clock:
- Watchdog Timer (WWDT)
- Real-Time Clock (RTC)
- 15-bit interval timer
- Timer TimerA

5.5.4 PLL Clock

- PLL: Can be used as the system clock. The PLL can select an external clock from the source clock or an internal high-speed oscillator clock.

5.6 Power Management

5.6.1 Power Supply Mode

V_{DD}: External power supply with a voltage range of 2.0 to 5.5V.
EV_{DD}: External power supply with a voltage range of 2.0 to 5.5V.
The voltage at the V_{DD} pin must be equal to the voltage at the EV_{DD} pin.

5.6.2 Power-on Reset

The power-on reset circuit (POL) has the following functions.

- An internal reset signal is generated when the power is turned on. If the supply voltage (V_{DD}) is greater than the sense voltage (V_{POL}), the reset is released. However, the reset state must be maintained by voltage detection circuitry or an external reset before the operating voltage range is reached.
- Drag the supply voltage (V_{DD}) and detection voltage (V_{PDR}) to compare, when $V_{DD} < V_{PDR}$, an internal reset signal is generated. However, when the power supply drops, it must be transferred before it is less than the operating voltage range Deep sleepmode, or reset state via voltage detection circuit or external reset. If you want to restart the operation, you must confirm that the supply voltage has returned to the operating voltage range.

5.6.3 Voltage Detection

The voltage detection circuit sets the operating mode and sense voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) via option bytes. The voltage detection (LVD) circuit has the following functions:

- Comparing the supply voltage (V_{DD}) to the sense voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) generates an internal reset or interrupt request signal.
- The sense voltage of the supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by option bytes to select the sense level.
- Runs in deep sleep mode.
- When the power supply rises, the reset state must be maintained by voltage detection circuitry or external reset before reaching the operating voltage range. When the supply drops, it must be transferred to deep sleep mode before it is less than the operating voltage range, or set to reset by voltage detection circuitry or an external reset.
- The operating voltage range varies depending on the user option byte setting.

5.7 Low Power Mode

The BAT32A239 supports two low-power modes for the best compromise between low power consumption, short start-up times, and available wake-up sources:

- Sleep Mode: Enters sleep mode by executing sleep commands. Sleep mode is the mode that stops the CPU from running the clock. Each clock continues to oscillate if the high-speed system clock oscillation circuit, high-speed internal oscillator, or subsystem clock oscillation circuit is oscillating before setting sleep mode. Although this mode does not allow the operating current to drop to the level of deep sleep mode, it is an effective mode when you want to restart processing immediately with an interrupt request or if you want to do intermittent operation frequently.
- Deep Sleep Mode: Enter Deep Sleep Mode by executing the Deep Sleep command. Deep sleep mode is a mode that stops the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stops the entire system. It can greatly reduce the operating current of the chip. Because deep sleep mode can be lifted by interrupt requests, it can also be run intermittently. However, in the case of the X1 clock, because the wait time to ensure oscillation stability is required when the deep sleep mode is released, it is necessary to select the sleep mode if it is necessary to start processing immediately with an interrupt request.

In either mode, the registers, flags, and data memory all remain in the pre-standby mode setting, and also maintain the state of the output latches and output buffers of the input/output ports.

5.8 Reset Function

The following 7 methods generate a reset signal.

1) Input external reset via the RESETB pin.
2) Internal reset is generated by program runaway detection of the watchdog timer.
3) An internal reset is generated by comparing the supply voltage and the sense voltage of the power-on reset (POR) circuit.
4) An internal reset is generated by comparing the supply voltage and the sense voltage of the voltage detection circuit (LVD).
5) Internal reset due to RAM parity error.
6) Internal reset due to access to illegal memory.
7) Software reset

Internal reset is the same as external reset, and after the reset signal is generated, the program is executed from the addresses written in addresses 0000H and 0001H.

5.9 Interrupt Function

The Cortex-M0+ processor has a built-in Nested Vector Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs, as well as one non-maskable interrupt (NMI) input, as well as multiple internal exceptions.

This product extends 32 maskable interrupt requests (IRQs) and 1 non-maskable interrupt (NMI) to support up to 96 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies by product.

		48 pins	64 pins	80 pins
Interrupts can be masked	external	11	12	12
	internal	33	33	44

5.10 Real-time Clock (RTC).

The real-time clock (RTC) has the following functions.

- Counters with year, month, day, day, hour, minute, and second.
- Fixed cycle interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month).
- Alarm interrupt function (alarm: week, hour, minute)
- 1Hz pin output function
- Supports crossover of the secondary system clock or master system clock as the operating clock of the RTC
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up in deep sleep mode
- Supports a wide range of clock correction functions

Year, month, day, hour, minute, and second counts can only be performed if the secondary system clock (32.768kHz) or the crossover of the primary system clock is selected as the operating clock of the RTC. When a low-speed internal oscillator clock (15kHz) is selected, only a fixed-cycle interrupt function can be used.

5.11 Watchdog Timer

1-channel WWDT, 17bit watchdog timer runs with option byte setting count. The watchdog timer operates with a low-speed internal oscillator clock (15kHz). A watchdog timer is used to detect a program that is out of control. When a program runaway is detected, an internal reset signal is generated.

The following situations are judged to be out of control of the program:

- When the watchdog timer counter overflows
- When performing a 1-bit operation instruction on the Allow Register (WDTE) of the watchdog timer
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register while the window is closed

5.12 SysTick Timer

This timer is dedicated to RTOS, but can also be used as a standard decrement counter.

It features a 24-bit decreasing counter with a self-loading capacity counter that generates a shieldable system interrupt when the self-loading capacity counter reaches 0.

5.13 Timer Timer4

This product contains timer unit Timer4 with four 16-bit timers. Each 16-bit timer is called a "channel" and can be used as a separate timer or as a combination of multiple channels for advanced timer functionality.

For details of each feature, please refer to the following table.

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counters ● Crossover ● Measurement of input pulse intervals ● Measurement of the high/low level width of the input signal ● Latency counters	● Single trigger pulse output ● PWM output ● Multiple PWM outputs

5.13.1 Independent Channel Operation Function

The independent channel operation function is a function that can use any channel independently of other channel operating modes. The stand-alone channel operation function can be used as the following modes:

1) Interval Timer: Can be used as a reference timer for interrupting at fixed intervals (INTTMs).
2) Square Wave Output: Whenever an INTTM interrupt is generated, a flip is triggered to output a square wave of 50% duty cycle from the timer output pin (TO).
3) External Event Counter: Counts the effective edge of the input signal at the timer input pin (TI) and can be used as an event counter to generate an interrupt if a specified number of times are reached.
4) Divider function (Channel 0 of unit 0 only): The input clock of the timer input pin (TI00) is divided and then output from the output pin (TO00).
5) Measurement of input pulse interval: The interval between input pulses is measured by counting at the effective edge of the input pulse signal at the timer input pin (TI) and the effective edge of the next pulse is captured with the count value.
6) Measurement of the high/low width of the input signal: The width of the input signal is measured by counting at one edge of the input signal at the timer input pin (TI) and capturing the count value on the other edge.
7) Delay Counter: The active edge of the input signal at the timer input pin (TI) begins to count and generates an interrupt after any delay period has elapsed.

5.13.2 Multi-channel Linkage Operation Function

The multi-channel linkage operation function can combine the functions implemented by combining the master channel (the reference timer for the main control period) and the slave channel (the timer that operates in accordance with the main control channel). The multi-channel linkage operation function can be used as the following modes:

1) Single-trigger pulse output: Two channels are used in pairs to generate a single-trigger pulse that arbitrarily sets the output timing and pulse width.
2) PWM (Pulse Width Modulation) output: 2 channels are used in pairs to generate pulses that can arbitrarily set the period and duty cycle.
3) Multiple PWM (Pulse Width Modulation) output: Up to 7 can be generated in fixed periods by extending the PWM function and using 1 master channel and multiple slave channels PWM signal for any duty cycle.

5.13.3 8-bit Timer Operation Function

The 8-bit timer run function uses a 16-bit timer channel as a function for two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

5.13.4 LIN-bus Support Functionality

The Timer4 unit can be used to check whether the received signal in LIN-bus communication is suitable for the LIN-bus communication format.

1) Detection of wake-up signals: The low width is measured by counting the beginning of the falling edge of the input signal at the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the width of the low level is greater than or equal to a fixed value, it is considered a wake-up signal.
2) Detection of the spacer field: After detecting a wake-up signal, the low level width is measured by counting from the falling edge of the input signal at the UART serial data input pin (RxD) and capturing the count value on the rising edge. If the low level width is greater than or equal to a fixed value, it is considered to be a spacer field.
3) Measurement of synchronous field pulse width: After detecting the interval field, measure the low and high width of the input signal of the UART serial data input pin (RxD). The baud rate is calculated based on the bit interval of the synchronous field measured in this way.

5.14 Timer Timer8

80-pin products add timer unit Timer8 with eight 16-bit timers. Each 16-bit timer is called a "channel" and can be used as a separate timer or as a combination of multiple channels for advanced timer functionality.

5.14.1 Independent Channel Operation Function

The independent channel operation function is a function that can use any channel independently of other channel operating modes. The stand-alone channel operation function can be used as the following modes:

1) Interval Timer: Can be used as a reference timer for interrupting at fixed intervals (INTTMs).
2) Square Wave Output: Whenever an INTTM interrupt is generated, a flip is triggered to output a square wave of 50% duty cycle from the timer output pin (TO).
3) External Event Counter: Counts the effective edge of the input signal at the timer input pin (TI) and can be used as an event counter to generate an interrupt if a specified number of times are reached.
4) Measurement of input pulse interval: The interval between input pulses is measured by counting at the effective edge of the input pulse signal at the timer input pin (TI) and the effective edge of the next pulse is captured with the count value.
5) Measurement of the high/low width of the input signal: The width of the input signal is measured by counting at one edge of the input signal at the timer input pin (TI) and capturing the count value on the other edge.
6) Delay Counter: The active edge of the input signal at the timer input pin (TI) begins to count and generates an interrupt after any delay period has elapsed.

5.14.2 Multi-channel Linkage Operation Function

The multi-channel linkage operation function can combine the functions implemented by combining the master channel (the reference timer for the main control period) and the slave channel (the timer that operates in accordance with the main control channel). The multi-channel linkage operation function can be used as the following modes:

1) Single-trigger pulse output: Two channels are used in pairs to generate a single-trigger pulse that arbitrarily sets the output timing and pulse width.
2) PWM (Pulse Width Modulation) output: 2 channels are used in pairs to generate pulses that can arbitrarily set the period and duty cycle.
3) Multiple PWM (Pulse Width Modulation) output: Up to 7 can be generated in fixed periods by extending the PWM function and using 1 master channel and multiple slave channels PWM signal for any duty cycle.

5.14.3 8-bit Timer Operation Function

The 8-bit timer run function uses a 16-bit timer channel as a function for two 8-bit timer channels. (Only Channel 1 and Channel 3 can be used).

5.15 Timer TimerA

This product contains a 16bit timer TimerA consisting of a reload register and a decrement counter. Available for the following modes of operation:

- Timer mode: Count the count source (the count source can be a clock or an external event)
- Pulse output mode: Counts the counting source and outputs the pulse in case of overflow
- Event Counting Mode: External events are counted and can work in deep sleep mode.
- Pulse Width Measurement Mode: The external pulse width is measured
- Pulse Period Measurement Mode: Measure the external pulse period

5.16 Timer TimerM

This product has a built-in 2-channel 16bit timer TimerM optimized for motor control, which has the following 4 operating modes:

- Timer mode:
  - Input capture function (triggered by an external signal to retrieve the count value to the register)
  - Output comparison function (detects whether the count value and register value are the same, and can change the output of the pin during the test)
  - PWM function (continuous output of arbitrary pulse width)
- Reset synchronous PWM mode: output sawtooth modulation, three-phase waveform without dead time (6 pcs)
- Complementary PWM mode: output triangular modulation, three-phase waveform with dead time (6 pcs)
- PWM3 Mode: Output Phase PWM Waveform (2 pcs)

5.17 Timer TimerB

This product has a built-in 16bit timer TimerB, which has the following 3 modes:

- Timer mode:
  - The input snap function counts on both sides of the rise, fall, or rise/fall edges.
  - Output comparison function "L" level output, "H" level output, or alternate output
- PWM mode: PWM output capable of any duty cycle.
- Phase counting mode: The count value of a 2-phase encoder can be measured automatically.

5.18 Timer TimerC

This product contains a 16 bit timer TimerC that can be triggered by software, comparator, or timer timerM for input capture.

5.19 15-bit Interval Timer

A built-in 15-bit interval timer generates interrupts (INTIT) at any pre-set interval that can be used to wake up from deep sleep mode.

5.20 Clock Output/Buzzer Output Control Circuitry

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. Clock output or buzzer output is implemented by a dedicated pin.

5.21 Universal Serial Communication Unit

This product has built-in 4 universal serial communication units, each unit has a maximum of 4 serial communication channels. Enables standard SPI, simple SPI, UART, and Simple I^2C communication functions. Taking the 80pin product as an example, the function allocation of each channel is as follows:

5.21.1 3-Wire Serial Interface (Simple SPI)

The serial clock (SCK) output of the master device transmits and receives data synchronously.

This uses 1 serial clock (SCK), 1 transmit serial data (SO), and 1 receive serial data (SI) for a total of 3 A clock-synchronous communication interface for communication lines to communicate.

[Send and receive data].

- 7-16 bits of data length
- Phase control of sending and receiving data
- MSB/LSB preferred choice

[Clock control].

- The choice of master or slave
- Phase control of the input/output clock
- The transfer period generated by the prescaler and the in-channel counter
- Maximum transfer rate

Master communication: Max. $F_{CLK}/2$

Slave communication: Max. $F_{MCK}/6$

[Interrupt function].

- End of transfer interrupt, buffer empty interrupt

[Error detection flag].

- Overflow error

5.21.2 SPI with Slave Chip Select

SPI serial communication interface supporting slave chip select input. This uses a slave chip select input (SSI), a serial clock (SCK), a transmit serial data (SO), and a receive serial data (SI) together Clock-synchronous communication interface for communication of 4 communication lines.

[Send and receive data].

- 7-16 bits of data length
- Phase control of sending and receiving data
- MSB/LSB preferred choice
- Level settings for sending and receiving data

[Clock control].

- Phase control of the input/output clock
- The transfer period generated by the prescaler and the in-channel counter
- Maximum transfer rate

Slave communication: Max. $F_{MCK}/6$

[Interrupt function].

- End of transfer interrupt, buffer empty interrupt

[Error detection flag].

- Overflow error

5.21.3 UART

The function of asynchronous communication through two lines of serial data transmission (TxD) and serial data receiving (RxD). Using these two communication lines, data is sent and received asynchronously (using the internal baud rate) with other communicating parties in a data frame (consisting of a start bit, data, parity bit, and stop bit). Full-duplex UART communication can be achieved by using two channels, send private (even channel) and receive private (odd channel), and LIN-bus can be supported by combining Timer4 unit and external interrupt (INTP0).

[Send and receive data].

- 7-bit, 8-bit, 9-bit, and 16-bit data length
- MSB/LSB preferred choice
- Level setting and inversion selection of transmitted and received data
- Additional parity functions for parity bits
- Attaching of stop bits, detection of stop bits

[Interrupt function].

- End of transfer interrupt, buffer empty interrupt
- Error interrupts caused by frame errors, parity errors, or overflow errors

[Error detection flag].

- Frame error, parity error, overflow error

[LIN-bus function].

- Detection of wake-up signals
- Detection of spaced field (BF).
- Measurement of the synchronous field, calculation of the baud rate

5.21.4 Simple I²C

The function of clock synchronization communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Because this simple I²C is designed for single communication with devices such as flash memory and A/D converters, it can only be used as a master device. The start and stop conditions, like the operating control registers, must comply with the AC characteristics and be handled by software.

[Send and receive data].

- Main control transmission, master receiving (limited to single main control master function)
- ACK output function Note, ACK detection function
- 8 bits of data length (when sending the address, specify the address with a height of 7 bits, and use the lowest bit for R/W control).
- Start and stop conditions are generated through software

[Interrupt function].

- The end of the transfer is interrupted

[Error detection flag].

- ACK error, overflow error

[Features not supported by Simple I²C].

- Slave send, slave receive
- Multi-master function (arbitration failure detection function)
- Wait for the detection function

5.22 Standard Serial Interface IICA

Serial interface IICA has the following 3 modes:

- Stop-Run mode: This is a mode used when no serial transfer is taking place, which reduces power consumption.
- I^2C bus mode (multi-master supported): This mode transfers 8-bit data to multiple devices via two wires of the serial clock (SCLA) and the serial data bus (SDAA). In accordance with the I^2C-bus format, the master device can generate "start conditions", "addresses", " for the slave devices on the serial data bus, "address", " Indication of the direction of transmission", "Data" and "Stop condition". The slave automatically detects the received status and data through the hardware. This feature simplifies the I^2C-bus control portion of the application. Because the SCLA and SDAA pins of the serial interface IICA are used as open-drain outputs, the serial clock line and serial data bus require pull-up resistors.
- Wake-up mode: In deep sleep mode, deep sleep mode can be released by generating an interrupt request signal (INTIICA) when receiving the extension code or local station address of the autonomous control device. This is set via the IICA control register.

5.23 Controller CAN

Universal CAN controller interface function in accordance with the CAN protocol in accordance with the standard in ISO 11898.

- Compliant with ISO 11898 and tested in accordance with ISO/DIS 16845 (CAN Conformity).
- Use standard frames and extended frames to implement receive and send
- Communication speed: maximum 1Mbps. (CAN input clock greater than or equal to 8MHz)
- 1 channel has 16 message caches
- Receive/send history list function
- Automatic block transfer function
- Multi-cache receive block capability
- Masking settings for four modes per channel

5.24 Analog-to-digital Converters (ADCs).

This product contains a 12-bit resolution analog-to-digital converter SARADC, which converts analog inputs to digital values, and supports up to 21 channels of ADC analog inputs (ANI0 to ANI20). The ADC contains the following features:

- 12-bit resolution, slew rate 1.42Msps.
- Trigger mode: Support software trigger, hardware trigger and hardware trigger in standby
- Channel selection: Supports two modes: single-channel selection and multi-channel scanning
- Conversion mode: Supports single conversion and continuous conversion
- Operating voltage: Supports 2.0V ≤ V_{DD} ≤ 5.5V operating voltage range
- Senses the built-in reference voltage (1.45V) and temperature sensor.

The ADC can set various A/D conversion modes using the combination of modes described below.

Trigger mode	Software triggered	Start the conversion with software operation.
	Hardware triggers no-wait	Start the conversion by detecting a hardware trigger.
	The hardware triggers the wait mode	In power-off transition standby, power is plugged in by detecting a hardware trigger and the transition automatically begins after the A/D power stabilization wait time.
Channel selection mode	Select the mode	Select 1 channel of analog inputs for A/D conversion.
	Scan mode	A/D conversion of analog inputs for 4 channels sequentially. Four consecutive channels from ANI0 to ANI15 can be selected as analog
Conversion mode	Single conversion mode	Performs 1 A/D conversion on the selected channel.
	Continuous conversion mode	Continuous A/D conversion of the selected channel until stopped by the software.
Sample time/conversion time	Number of sample clocks/conversion clocks	The sample time can be set by registers, with the default value of 13.5 clk for the number of sample clocks and 31.5 clk for the number of converted clocks.

5.25 Digital-to-analog Converters (DAC)

This product contains a 2-channel 8-bit resolution analog-to-digital converter DAC that converts digital inputs to analog signals. Has the following characteristics:

- 8-bit resolution D/A converter
- Supports the outputs of two independent analog channels
- R-2R ladder network
- Built-in real-time output function

5.26 Programmable Gain Amplifier (PGA)

Two programmable gain amplifiers (PGA0 and PGA1) are included in this product with the following functions

- There are 7 options for amplification gain per PGA: 4x, 8x, 10x, 12x, 14x, 16x, 32x
- An external pin can be selected as ground for the PGA negative feedback resistor (available as differential mode).
- The output of PGA0 can be selected as an analog input for an A/D converter or as an analog input at the positive end of Comparator 0 (CMP0).
- The output of PGA1 can be selected as an analog input for A/D converters

5.27 Comparators (CMP)

This product has built-in two-channel comparators CMP0 and CMP1 with the following functions:

- External input and reference multi-channel options for CMP1.
- An external reference input and an internal reference voltage can be selected for the reference.
- The cancellation width of the noise cancellation digital filter can be selected.
- Detects the active edge of the comparator output and generates an interrupt signal.
- Detects the active edge of the comparator output and outputs the event signal to the linkage controller.

5.28 Two-wire Serial Debug Port (SW-DP)

ARM's SW-DP interface allows connection to a microcontroller via a serial line debugging tool.

5.29 Security Features

5.29.1 Flash CRC Computing Functions (High-speed CRC, General-purpose CRC)

Detect data errors in flash memory by CRC operation.

The following two CRCs can be used according to different uses and conditions of use.

- High-speed CRC: In the initialization program, it can stop the operation of the CPU and check the entire code flash memory area at high speed.
- Generic CRC: In CPU operation, it is not limited to the flash memory area of the code but can be used for multi-purpose inspection.

5.29.2 RAM Parity Error Detection Function

When reading RAM data, parity errors are detected.

5.29.3 SFR Protection Features

Prevent important SFRs (Special Function Registers) from being overwritten due to CPU runaways.

5.29.4 Illegal Memory Access Detection Function

Detects illegal access to illegal memory areas (areas without memory or areas with restricted access).

5.29.5 Frequency Detection Function

Self-test CPU or peripheral hardware clock frequency using Timer4 units.

5.29.6 A/D Testing Capabilities

The A/D is converted to the A/D converter's positive (+) reference, negative (-) reference, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage. The converter performs self-test.

5.29.7 Digital Output Signal Level Detection Function for Input/Output Ports

When the input/output ports are in output mode, the output level of the pin can be read.

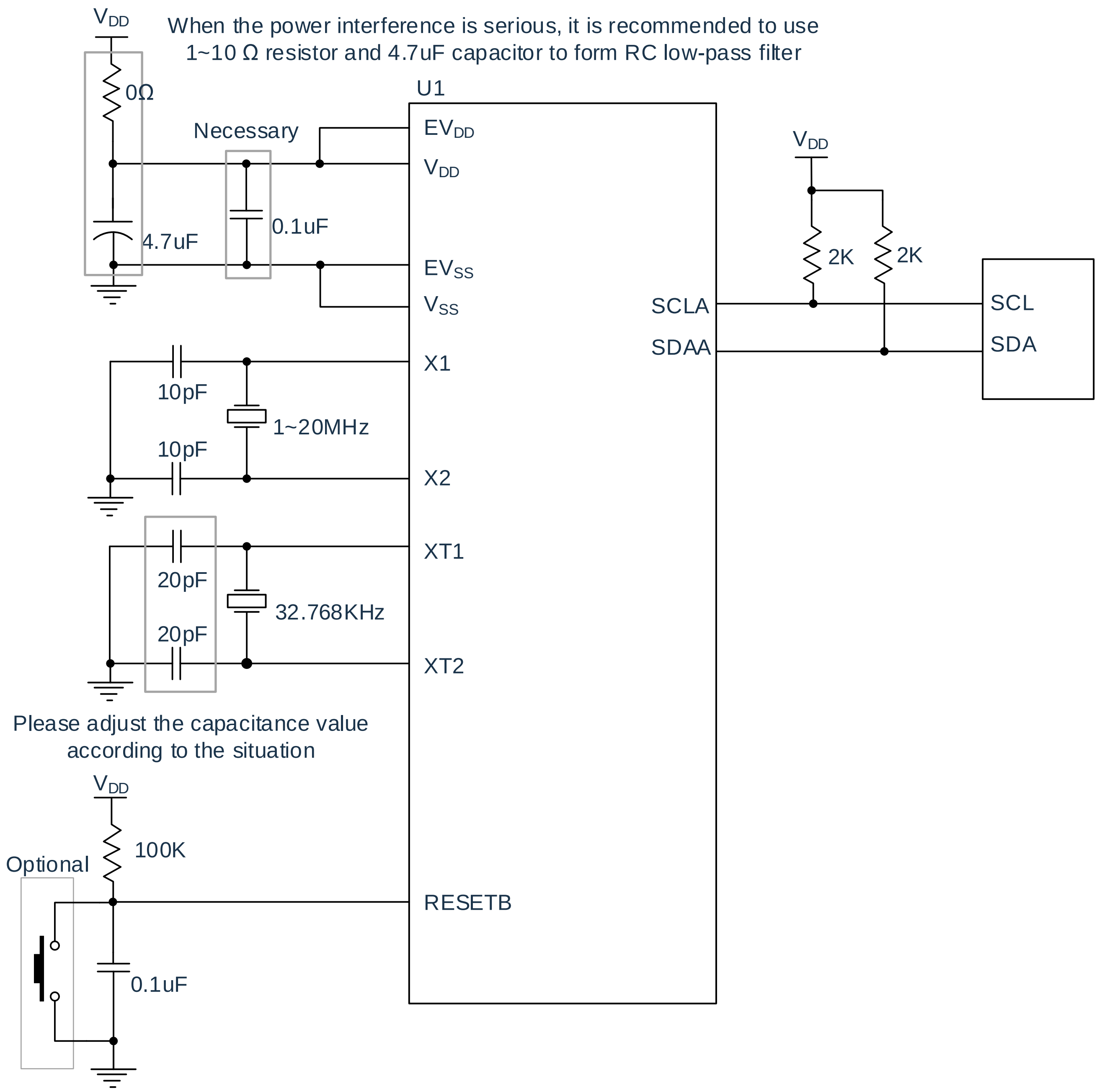
5.30 Key Function

A key interrupt (INTKR) can be generated by pressing the key interrupt input pin (KR0 to KR7) to enter the falling edge.

6 Electrical Characteristics

6.1 Typical Application of Peripheral Circuits

Device connections for typical MCU application peripheral circuits refer to the following:



6.2 Absolute Maximum Voltage Rating

(T_A= -40~125°C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	-	-0.5~+6.5	V
	EV_{DD}	-	-0.5~+6.5	V
Input voltage	V_{I1}	P00~P06, P10~P17, P30, P31, P40~P45 P50~P55, P64~P67, P70~P77, P100 P110~P111, P120, P136, P140~P144 P146~P147, P150~P153	-0.3~EV_{DD} +0.3 and -0.3~V_{DD} +0.3 Note1	V
	V_{I2}	P60~P63(N-channel drain open)	-0.3~+6.5	V
	V_{I3}	P20~P27, P121~P124, P137, EXCLK EXCLKS, RESETB	-0.3~V_{DD} +0.3 Note1	V
Output voltage	V_{O1}	P00~P06, P10~P17, P30, P31, P40~P45 P50~P55, P60~P67, P70~P77, P100 P110~P111, P120, P136, P140~P144 P146~P147, P150~P153	-0.3~EV_{DD} +0.3 and -0.3~V_{DD} +0.3 Note1	V
	V_{O2}	P20~P27, P137	-0.3~V_{DD} +0.3 Note1	V
Analog input voltage	V_{AI1}	ANI8~ANI20	-0.3~EV_{DD} +0.3 and -0.3~AV_{REF}(+)+0.3 Note1,2	V
	V_{AI2}	ANI0~ANI7	-0.3~V_{DD} +0.3 and -0.3~AV_{REF}(+)+0.3 Note1,2	V

Note1: Not to exceed 6.5V.

Note2: The pin of the A/D conversion object cannot exceed AV_{REF}(+)+0.3.

Note: Even if 1 item in each project exceeds the absolute maximum rating instantaneously, the quality of the product may be reduced. The absolute maximum rating is the rating that may cause physical damage to the product and must be used in a state that does not exceed the rated value.

Remark:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. AV_{REF}(+): The positive (+) reference voltage of the A/D converter
3. Use V_{SS} as the reference voltage.
4. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

6.3 Absolute Maximum Current Rating

(T_A= -40~125˚C)

<table>
<tr><th>Item</th><th>Symbol</th><th colspan="2">Condition</th><th>Rating</th><th>Unit</th></tr>
<tr><td rowspan="5">High output current</td><td rowspan="3">I_{OH1}</td><td>Each pin</td><td>P00~P06, P10~P17, P30, P31, P40~P45, P50~P55
P64~P67, P70~P77, P100, P110~P111, P120, P130
P136, P137, P140~P144, P146~P147, P150~P153</td><td>-40</td><td>mA</td></tr>
<tr><td rowspan="2">Total pins - 170mA</td><td>P00~P04, P40~P45, P120, P130, P136, P137
P140~P144, P150~P153</td><td>-70</td><td>mA</td></tr>
<tr><td>P05, P06, P10~P17, P30, P31, P50~P55, P64~P67
P70~P77, P100, P110~P111, P146, P147</td><td>-100</td><td>mA</td></tr>
<tr><td rowspan="2">I_{OH2}</td><td>Each pin</td><td rowspan="2">P20~P27</td><td>-3</td><td>mA</td></tr>
<tr><td>Total pins</td><td>-15</td><td>mA</td></tr>
<tr><td rowspan="5">Low output current</td><td rowspan="3">I_{OL1}</td><td>Each pin</td><td>P00~P06, P10~P17, P30, P31, P40~P45, P50~P55
P60~P67, P70~P77, P100, P110~P111, P120, P130
P136, P137, P140~P144, P146~P147, P150~P153</td><td>40</td><td>mA</td></tr>
<tr><td rowspan="2">The total pins are 170mA</td><td>P00~P04, P40~P45, P120, P130, P136, P137
P140~P144, P150~P153</td><td>100</td><td>mA</td></tr>
<tr><td>P05, P06, P10~P17, P30, P31, P50~P55, P60~P67
P70~P77, P100, P110~P111, P146, P147</td><td>120</td><td>mA</td></tr>
<tr><td rowspan="2">I_{OL2}</td><td>Each pin</td><td rowspan="2">P20~P27</td><td>15</td><td>mA</td></tr>
<tr><td>Total pins</td><td>45</td><td>mA</td></tr>
<tr><td rowspan="2">Operating ambient temperature</td><td rowspan="2">T_A</td><td colspan="2">Usually run</td><td rowspan="2">-40~125</td><td rowspan="2">˚C</td></tr>
<tr><td colspan="2">When flash programming</td></tr>
<tr><td>Storage temperature</td><td>T_{stg}</td><td colspan="2">-</td><td>-65~150</td><td>˚C</td></tr>
</table>

Note: Even if 1 item in each project exceeds the absolute maximum rating instantaneously, the quality of the product may be reduced. The absolute maximum rating is the rating that may cause physical damage to the product and must be used in a state that does not exceed the rated value.

Remark:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

6.4 Oscillation Circuit Characteristics

6.4.1 X1, XT1 Features

(T_A= -40~125℃,2.0V≤V_{DD}≤5.5V,V_{SS}=0V)

Item	Resonators	Condition	Min	Typ	Max	Unit
X1 clock oscillation frequency (F_X).	Ceramic resonator/crystal resonator	-	1.0	-	20.0	MHz
X1 clock oscillation settling time	Ceramic resonator/crystal resonator	20MHz,C=10pF	-	15	-	ms
X1 clock oscillation feedback resistor	Ceramic resonator/crystal resonator	-	0.6	-	1.8	MΩ
XT1 clock oscillation frequency (F_{XT}).	Crystal resonators	-	32	32.768	35	kHz
XT1 clock oscillation settling time	Crystal resonators	32.768kHz,C=20pF	-	2	-	s

Note:

1. It only indicates the frequency tolerance range of the oscillation circuit, and refer to the AC characteristics for the execution time of the instruction.
2. Please commission a resonator manufacturer to evaluate the installation circuit and use it after confirming the oscillation characteristics.
3. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

6.4.2 Internal Oscillator Features

(T_A= -40~125°C,2.0V≤V_{DD}≤5.5V,V_{SS}=0V)

Resonators	Condition	Min	Typ	Max	Unit
Clock frequency (F_{IH}) of the high-speed internal oscillator Note1,2	-	1.0	-	64.0	MHz
High-speed internal oscillator settling time (T_{SU}).	-	-	12	-	us
Clock frequency accuracy of a high-speed internal oscillator	T_A= 10~70°C	-1.0	-	+1.0	%
	T_A=0~105°C	-1.5	-	+1.5	%
	T_A= -10~125°C	-2.0	-	+2.0	%
	T_A= -40~125°C	-4.0	-	+4.0	%
The clock frequency (F_{IL}) of the low-speed internal oscillator	-	12	15	18	KHz

Note:

1. Select the frequency of the high-speed internal oscillator via the option byte.
2. Indicates only the characteristics of the oscillation circuit, please refer to the AC characteristics for the execution time of the instruction.

Remark: Low temperature specification value shall be guaranteed by the design, and low temperature conditions shall not be measured in mass production.

6.4.3 PLL Oscillator Characteristics

(T_A= -40~125°C,2.0V≤V_{DD}≤5.5V,V_{SS}=0V)

Resonators	Condition	Min	Typ	Max	Unit
PLL input frequency Note1	-	4.0	-	8.0	MHz
PLL lock time	-	40	-	-	ms

Note1: Only the characteristics of the oscillation circuit are indicated, please refer to the AC characteristics for the execution time of the instruction

Remark: Low temperature specification value shall be guaranteed by the design, and low temperature conditions shall not be measured in mass production.

6.5 DC Characteristics

6.5.1 Pin Characteristics

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Project	Symbol	Condition		Min	Typ	Max	Unit
High output current Note1	I_{OH1}	P00~P06, P10~P17, P30, P31 P40~P45, P50~P55, P64~P67 P70~P77, P100, P110~P111 P120, P130, P136, P137 P140~P144, P146~P147 P150~P153 1 pin alone	2.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-12.0Note2	mA
			2.0V≤EV_{DD}≤5.5V 85~125℃	-	-	-6.0Note2	
		P00~P04, P40~P45, P120 P130, P136, P137 P140~P144, P150~P153 Total pins (at duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-60.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-12.0	mA
			2.0V≤EV_{DD}<2.4V	-	-	-6.0	mA
		P05, P06, P10~P17, P30, P31 P50~P55, P64~P67, P70~P77 P100, P110~P111 P146, P147Total pins (at duty cycle ≤ 70% Note3).	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-80.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	-30.0	
			2.4V≤EV_{DD}<4.0V	-	-	-20.0	mA
			2.0V≤EV_{DD}<2.4V	-	-	-10.0	mA
		Total pins (at duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85℃	-	-	-140.0	mA
			4.0V≤EV_{DD}≤5.5V 85~125℃	-	-	-60.0	
			2.4V≤EV_{DD}≤4.0V	-	-	-30.0	
			2.0V≤EV_{DD}≤2.4V	-	-	-15.0	
	I_{OH2}	P20~P27 1 pin alone	2.0V≤V_{DD}≤5.5V	-	-	-2.5 Note2	mA
		Total pins (at duty cycle ≤ 70% Note3)	2.0V≤V_{DD}≤5.5V	-	-	-10	mA

Note1: This is the current value that guarantees the operation of the device even if the current flows from the EV_{DD} and V_{DD} pins to the output pins.

Note2: The total current value cannot be exceeded.

Note3: This is the output current value for the "duty cycle ≤70% condition". The output current value >of 70% can be calculated using the following calculation method (if the duty cycle is changed to n%).

Total output current of pins = (I_{OH}×0.7)/(n×0.01).

＜calculation example＞I_{OH} = -10.0mA,n =80%

Total output current of pins = (-10.0×0.7)/(80×0.01) ≈-8.7mA

The current at each pin does not vary due to duty cycle and does not flow above the absolute maximum rating.

Note: In N-channelopen-drain mode, pins set to active N-channel open-drain do not output high.

Remarks:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. Low temperature specification value shall be guaranteed by the design, and low temperature conditions shall not be measured in mass production.

(T_A= -40~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Project	Symbol	Condition		Min	Typ	Max	Unit
Low output current Note1	I_{OL1}	P00~P06, P10~P17, P30, P31 P40~P45, P50~P55, P60~P67 P70~P77, P100, P110~P111, P120 P130, P136, P137, P140~P144 P146~P147, P150~P153 1 pin alone	2.0V≤EV_{DD}≤5.5V -40~85°C	-	-	30 Note2	mA
			2.0V≤EV_{DD}≤5.5V 85~125°C	-	-	15 Note2	
		P00~P04, P40~P45, P120, P130 P136, P137, P140~P144, P150~P153 Total pins (at duty cycle ≤ 70% Note3).	4.0V≤EV_{DD}≤5.5V -40~85°C	-	-	100	mA
			4.0V≤EV_{DD}≤5.5V 85~125°C	-	-	50	
			2.4V≤EV_{DD}<4.0V	-	-	30	mA
			2.0V≤EV_{DD}<2.4V	-	-	15	mA
		P05, P06, P10~P17, P30, P31 P50~P55, P60~P67, P70~P77, P100 P110~P111, P146, P147 Total pins (at duty cycle ≤ 70% Note3).	4.0V≤EV_{DD}≤5.5V -40~85°C	-	-	120	mA
			4.0V≤EV_{DD}≤5.5V 85~125°C	-	-	60	
			2.4V≤EV_{DD}<4.0V	-	-	40	mA
			2.0V≤EV_{DD}<2.4V	-	-	20	mA
		Total pins (at duty cycle ≤ 70% Note3)	4.0V≤EV_{DD}≤5.5V -40~85°C	-	-	150	mA
			4.0V≤EV_{DD}≤5.5V 85~125°C	-	-	80	
			2.4V≤EV_{DD}≤4.0V	-	-	50	
			2.0V≤EV_{DD}≤2.4V	-	-	30	
	I_{OL2}	P20~P27 1 pin alone	2.0V≤V_{DD}≤5.5V	-	-	6 Note2	mA
		Total pins (at duty cycle ≤ 70% Note3)	2.0V≤V_{DD}≤5.5V	-	-	20	mA

Note1: This is the current value that guarantees the operation of the device even if the current flows from the output pin to the EV_{SS} and V_{SS} pins.

Note2: The total current value cannot be exceeded.

Note3: This is the output current value for the "duty cycle ≤70% condition". The output current value of 70% is changed to duty cycle>can be calculated using the following calculation (if the duty cycle is changed to n%).

Total output current = (I_{OL}×0.7)/(n×0.01).

<calculation example>I_{OL}= 10.0mA,n = 80%

Total Output Current = (10.0×0.7)/(80×0.01) ≈ 8.7mA Each pin does not vary due to duty cycle and does not flow above the absolute maximum rating.

Note:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. Low temperature specification value shall be guaranteed by the design, and low temperature conditions shall not be measured in mass production.

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Project	Symbol	Condition		Min	Typ	Max	Unit
Power supply input voltage	V_{DD} EV_{DD}	-		2.0	-	5.5	V
The supply ground input voltage	V_{SS} EV_{SS}	-		-0.3	-	-	V
High input voltage	V_{IH1}	P00~P06, P10~P17, P30, P31 P40~P45, P50~P55, P64~P67 P70~P77, P100, P110~P111 P120, P136, P140~P144 P146~P147, P150~P153	Schmidt input	0.8EV_{DD}	-	EV_{DD}	V
	V_{IH2}	P01, P03, P04, P10, P14~P17 P30, P43~P44, P50, P55 P142~P143	TTL input 4.0V≤EV_{DD}≤5.5V	2.2	-	EV_{DD}	V
			TTL input 3.3V≤EV_{DD}<4.0V	2.0	-	EV_{DD}	V
			TTL input 2.0V≤EV_{DD}<3.3V	1.5	-	EV_{DD}	V
	V_{IH3}	P20~P27, P137		0.7V_{DD}	-	V_{DD}	V
	V_{IH4}	P60~P63		0.7EV_{DD}	-	6.0	V
	V_{IH5}	P121~P124, EXCLK, EXCLKS, RESETB		0.8V_{DD}	-	V_{DD}	V
Low input voltage	V_{IL1}	P00~P06, P10~P17, P30, P31 P40~P45, P50~P55, P64~P67 P70~P77, P100, P110~P111 P120, P136, P140~P144 P146~P147, P150~P153	Schmidt input	0	-	0.2EV_{DD}	V
	V_{IL2}	P01, P03, P04, P10, P14~P17 P30, P43~P44, P50, P55 P142~P143	TTL input 4.0V≤EV_{DD}≤5.5V	0	-	0.8	V
			TTL input 3.3V≤EV_{DD}<4.0V	0	-	0.5	V
			TTL input 2.0V≤EV_{DD}<3.3V	0	-	0.32	V
	V_{IL3}	P20~P27, P137		0	-	0.3V_{DD}	V
	V_{IL4}	P60~P63		0	-	0.3EV_{DD}	V
	V_{IL5}	P121~P124, EXCLK, EXCLKS, RESETB		0	-	0.2V_{DD}	V

Note: Even N-channel open-drain mode, the V_{IH} maximum (MAX.) of the pin set to active N-channel open-drain is EV_{DD}.

Remark:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

(T_A= -40 ~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Project	Symbol	Condition		Min	Typ	Max	Unit
High output voltage	V_{OH1}	P00~P06, P10~P17, P30 P31, P40~P45, P50~P55 P64~P67, P70~P77, P100 P110~P111, P120, P130 P136, P137, P140~P144 P146~P147, P150~P153	4.0V≤EV_{DD}≤5.5V, I_{OH1}= -12.0mA	EV_{DD}-1.5	-	-	V
			4.0V≤EV_{DD}≤5.5V, I_{OH1}= -6.0mA	EV_{DD}-0.7	-	-	V
			2.4V≤EV_{DD}≤5.5V, I_{OH1}= -3.0mA	EV_{DD}-0.6	-	-	V
			2.0V≤EV_{DD}≤5.5V, I_{OH1}= -2mA	EV_{DD}-0.5	-	-	V
	V_{OH2}	P20~P27	4.0V≤V_{DD}≤5.5V, I_{OH2}= -2.5mA	EV_{DD}-1.5	-	-	V
			4.0V≤V_{DD}≤5.5V, I_{OH2}= -1.5mA	EV_{DD}-0.7	-	-	V
			2.4V≤V_{DD}≤5.5V, I_{OH2}= -0.5mA	EV_{DD}-0.6	-	-	V
			2.0V≤V_{DD}≤5.5V, I_{OH2}= -0.4mA	V_{DD}-0.5	-	-	V
Low output voltage	V_{OL1}	P00~P06, P10~P17, P30 P31, P40~P45, P50~P55 P60~P67, P70~P77, P100 P110~P111, P120, P130 P136, P137, P140~P144 P146~P147, P150~P153	4.0V≤EV_{DD}≤5.5V, I_{OL1}=30.0mA	-	-	1.2	V
			4.0V≤EV_{DD}≤5.5V, I_{OL1}=15.0mA	-	-	0.7	V
			2.4V≤EV_{DD}≤5.5V, I_{OL1}=6.0mA	-	-	0.4	V
			2.0V≤EV_{DD}≤5.5V, I_{OL1}=4.0mA	-	-	0.4	V
	V_{OL2}	P20~P27	4.0V≤V_{DD}≤5.5V, I_{OL2}=6.0mA	-	-	1.2	V
			4.0V≤V_{DD}≤5.5V, I_{OL2}=4.0mA	-	-	0.7	V
			2.4V≤V_{DD}≤5.5V, I_{OL2}=1.5mA	-	-	0.4	V
			2.0V≤V_{DD}≤5.5V, I_{OL2}=1.0mA	-	-	0.4	V

Note: Even N-channel open-drain mode, pins set to active N-channel open-drain do not output high.

Remark:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Project	Symbol	Condition		Min	Typ	Max	Unit
High input leakage current	I_{LIH1}	P00~P06, P10~P17, P30, P31 P40~P45, P50~P55, P60~P67 P70~P77, P100, P110~P111 P120, P130, P136 P140~P144, P146~P147 P150~P153	V_I=EV_{DD}	-	-	1	uA
	I_{LIH2}	P20~P27, P137, RESETB	V_I=V_{DD}	-	-	1	uA
	I_{LIH3}	P121~P124(X1, X2, EXCLK XT1, XT2, EXCLKS)	V_I=V_{DD}, when the input port and external clock are in	-	-	1	uA
			V_I=V_{DD}, when a resonator is connected	-	-	10	uA
Low input leakage current	I_{LIL1}	P00~P06, P10~P17, P30, P31 P40~P45, P50~P55, P60~P67 P70~P77, P100, P110~P111 P120, P130, P136 P140~P144, P146~P147 P150~P153	V_I=EV_{SS}	-	-	-1	uA
	I_{LIL2}	P20~P27, P137, RESETB	V_I=V_{SS}	-	-	-1	uA
	I_{LIL3}	P121~P124(X1, X2, EXCLK XT1, XT2, EXCLKS)	V_I=V_{SS}, when the input port and external clock are in	-	-	-1	uA
			V_I=V_{SS}, when a resonator is connected	-	-	-10	uA
Internal pull-up resistor	R_U	P00~P06, P10~P17, P30, P31 P40~P45, P50~P55, P64~P67 P70~P77, P100, P110~P111 P120, P136, P137 P140~P144, P146~P147	V_I=EV_{SS},when entering the port	10	30	100	KΩ

Note:

1. Unless specifically specified, the characteristics of the multiplexed pin are the same as those of the port pin.
2. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

6.5.2 Supply Current Characteristics

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Project	Symbol	Condition				Min	Typ	Max	Unit
Supply current Note1	I_{DD1}	Run mode	High-speed internal oscillator	F_{HOCO}=64MHz,F_{IH}=64MHz Note3		-	7.6	15	mA
				F_{HOCO}=48MHz,F_{IH}=48MHz Note3		-	7.0	12	
				F_{HOCO}=32MHz,F_{IH}=32MHz Note3		-	6.0	10	
			High-speed master system	F_{MX}=20MHz Note2	Input square wave	-	4.0	8.0	mA
					Connecting crystal oscillator	-	4.0	8.0	
			The secondary system clock runs	F_{SUB}=32.768KHz Note4	Input square wave	-	70	150	uA
					Connecting crystal oscillator	-	70	150	
	I_{DD2}	Sleep mode	High-speed internal oscillator	F_{HOCO}=64MHz,F_{IH}=64MHz Note3		-	2.0	7.8	mA
				F_{HOCO}=48MHz,F_{IH}=48MHz Note3		-	1.6	6.5	
				F_{HOCO}=32MHz,F_{IH}=32MHz Note3		-	1.2	4.5	
			High-speed master system	F_{MX} =20MHz Note2	Input square wave	-	0.7	3.2	mA
					Connecting crystal oscillator	-	0.7	3.2	
			The secondary system clock runs	F_{SUB}=32.768KHz Note5	Input square wave	-	1.2	60	uA
					Connecting crystal oscillator	-	1.2	60	
	I_{DD3} Note6	Deep sleep mode Note7	T_A = -40℃~25℃ V_{DD}=3.0V			-	0.8	1.4	uA
			T_A = -40℃~85℃ V_{DD}=3.0V			-	0.8	15	
			T_A = -40℃~105℃ V_{DD}=3.0V			-	0.8	22	
			T_A = -40℃~125℃ V_{DD}=3.0V			-	0.8	55	

Note1: This is the total current flowing through V_{DD} and EV_{DD}, including input pins fixed as V_{DD}, EV_{DD} or V_{SS}, EV_{SS} The input leakage current of the state. TYP. Value: The CPU is in multiplication instruction execution (I_{DD1}) and does not contain peripheral operating current. MAX.Value: The CPU is in multiplication instruction execution (I_{DD1}) and contains peripheral operating current, but does not contain current flowing to the A/D converter, LVD circuitry, I/O port, and internal pull-up or pull-down resistors. It also does not include the current at which the data flash is overwritten.

Note2: This is a case where the high-speed internal oscillator and the subsystem clock stop oscillating.

Note3: This is when the high-speed master system clock and the secondary system clock stop oscillating.

Note4: This is a case where the high-speed internal oscillator and the high-speed master system clock stop oscillating.

Note5: This is a case where the high-speed internal oscillator and the high-speed master system clock stop oscillating. Contains current flowing to the RTC, but does not flow to the 15-bit interval timer and watchdog The current of the timer.

Note6: Does not include current to RTCs, 15-bit interval timers, and watchdog timers.

Note7: For current values when the secondary system clock is running in deep sleep mode, refer to the current value when the secondary system clock is running in sleep mode.

Remark:

1. F_{HOCO}: Clock frequency of high-speed internal oscillator,
   F_{IH}: System clock frequency provided by high-speed internal oscillator.
2. F_{SUB}: External subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3. F_{MX}: External master system clock frequency (X1/X2 clock oscillation frequency).
4. TYP. The temperature condition of the value is T_A=25°C.
5. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Low-speed internal oscillator operating current	I_{FIL} Note1	-		-	0.2	-	uA
RTC operating current	I_{RTC} Note1,2,3	-		-	0.04	-	uA
15-bit interval timer operating current	I_{IT} Note1,2,4	-		-	0.02	-	uA
Watchdog timer operating current	I_{WDT} Note1,2,5	F_{IL}=15KHz		-	0.22	-	uA
The A/D converter operates current	I_{ADC} Note1,6	ADC HS mode@64MHz		-	2.2	-	mA
		ADC HS mode@4MHz		-	1.3	-	mA
		ADC LC mode@24MHz		-	1.1	-	mA
		ADC LC mode@4MHz		-	0.8	-	mA
The D/A converter operates current	I_{DAC} Note1,8	Per channel		-	1.4	-	mA
PGA operating current	-	Per channel		-	480	700	uA
Comparator operating current	I_{CMP} Note1,9	Per channel	The internal reference voltage is not used	-	60	100	uA
			An internal reference voltage is used	-	80	140	uA
LVD operating current	I_{LVD} Note1,7	-		-	0.08	-	uA

Note1: This is the current flowing through V_{DD}.

Note2: This is a case where the high-speed internal oscillator and the high-speed system clock stop oscillating.

Note3: This is the current that only flows to the real-time clock (RTC) (excluding the operating current of the low-speed internal oscillator and XT1 oscillation circuitry). With the real-time clock running in operating mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{RTC}. In addition, when selecting a low-speed internal oscillator, I_{FIL} must be added. I_{DD2} when the subsystem clock is running contains the operating current of the real-time clock.

Note4: This is the current that only flows to the 15-bit interval timer (excluding the operating current of the low-speed internal oscillator and the XT1 oscillation circuit). In the case of a 15-bit interval timer in operating mode or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{IT}. In addition, when selecting a low-speed internal oscillator, IFIL must be added.

Note5: This is the current that only flows to the watchdog timer (including the operating current of the low-speed internal oscillator). With the watchdog timer running, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{WDT}.

Note6: This is the current that only flows to the A/D converter. In either run mode or sleep mode with the A/D converter running, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{ADC}.

Note7: This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of I_{LVD}.

Note8: This is the current that only flows to the D/A converter. When the D/A converter is running in operating or sleep mode, the current value of the microcontroller is I_{DD1} or I_{DD2} plus the value of I_{DAC}.

Note9: This is the current that only flows to the comparator circuit. With the comparator circuit running, the current value of the microcontroller is I_{DD1} or I_{DD2} or I_{DD3} plus the value of the I_{CMP}.

Remark:

1. F_{IL} : The clock frequency of the low-speed internal oscillator
2. TYP. The temperature condition of the value is T_A = 25°C.
3. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

6.6 AC Characteristics

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Instruction period (minimum instruction execution time)	T_{CY}	The master system clock (F_{MAIN}) runs	2.0V≤V_{DD}≤5.5V	0.015625	-	1	us
		The secondary system clock (F_{SUB}) runs	2.0V≤V_{DD}≤5.5V	28.5	30.5	31.3	us
External system clock frequency	F_{EX}	2.0V≤V_{DD}≤5.5V		1.0	-	20.0	MHz
	F_{EXS}	2.0V≤V_{DD}≤5.5V		32.0	-	35.0	KHz
The high or low level width of the external system clock input	T_{EXH},T_{EXL}	2.0V≤V_{DD}≤5.5V		24	-	-	ns
	T_{EXHS},T_{EXLS}	2.0V≤V_{DD}≤5.5V		13.7	-	-	us
TI00 ~ TI03, TI10 ~ TI17 input high and low level width	T_{TIH},T_{TIL}	2.0V≤V_{DD}≤5.5V		1/F_{MCK}+10	-	-	ns
The input period of timer TimerA	T_C	TAIO	2.4V≤EV_{DD}≤5.5V	100	-	-	ns
			2.0V≤EV_{DD}<2.4V	300	-	-	ns
The high or low level width of the timer TimerA input	T_{TAIH},T_{TAIL}	TAIO	2.4V≤EV_{DD}≤5.5V	40	-	-	ns
			2.0V≤EV_{DD}<2.4V	120	-	-	ns

Note:

1. F_{MCK}: Timer4, Timer8 unit running clock frequency
2. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

<table>
<tr><th>Project</th><th>Symbol</th><th colspan="2">Condition</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>The high or low level width of the M input of the timer</td><td>T_{TMIH},T_{TMIL}</td><td colspan="2">TMIOA0, TMIOA1, TMIOB0, TMIOB1 TMIOC0, TMIOC1, TMIOD0, TMIOD1</td><td>3/F_{CLK}</td><td>-</td><td>-</td><td>ns</td></tr>
<tr><td rowspan="2">Timer M forces the cutoff of the low width of the signal input</td><td rowspan="2">T_{TMSIL}</td><td rowspan="2">P136/INTP0</td><td>2MHz<F_{CLK}≤48MHz</td><td>1</td><td>-</td><td>-</td><td>μs</td></tr>
<tr><td>F_{CLK} ≤ 2MHz</td><td>1/F_{CLK}+1</td><td>-</td><td>-</td><td>μs</td></tr>
<tr><td>The high and low level width of the timer B input</td><td>T_{TBIH},T_{TBIL}</td><td colspan="2">TBIOA,TBIOB</td><td>2.5/F_{CLK}</td><td>-</td><td>-</td><td>ns</td></tr>
<tr><td rowspan="3">TO00 ~ TO03, TO10 ~ TO17, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOB output frequency</td><td rowspan="3">F_{TO}</td><td colspan="2">4.0V≤EV_{DD}≤5.5V</td><td>-</td><td>-</td><td>16</td><td>MHz</td></tr>
<tr><td colspan="2">2.4V≤EV_{DD}<4.0V</td><td>-</td><td>-</td><td>8</td><td>MHz</td></tr>
<tr><td colspan="2">2.0V≤EV_{DD}<2.4V</td><td>-</td><td>-</td><td>4</td><td>MHz</td></tr>
<tr><td rowspan="3">Output frequencies of CLKBUZ0 and CLK BUZ1</td><td rowspan="3">F_{PCL}</td><td colspan="2">4.0V≤EV_{DD}≤5.5V</td><td>-</td><td>-</td><td>16</td><td>MHz</td></tr>
<tr><td colspan="2">2.4V≤EV_{DD}<4.0V</td><td>-</td><td>-</td><td>8</td><td>MHz</td></tr>
<tr><td colspan="2">2.0V≤EV_{DD}<2.4V</td><td>-</td><td>-</td><td>4</td><td>MHz</td></tr>
<tr><td>The high and low level width of the interrupt input</td><td>T_{INTH},T_{INTL}</td><td>INTP0 ~ INTP11</td><td>2.0V≤EV_{DD}≤5.5V</td><td>1</td><td>-</td><td>-</td><td>μs</td></tr>
<tr><td>The key interrupts the high or low level width of the input</td><td>T_{KR}</td><td>KR0 ~ KR7</td><td>2.0V≤EV_{DD}≤5.5V</td><td>250</td><td>-</td><td>-</td><td>ns</td></tr>
<tr><td>The low level width of RESETB</td><td>T_{RSL}</td><td colspan="2">-</td><td>10</td><td>-</td><td>-</td><td>μs</td></tr>
</table>

Note: The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured in mass production.

6.7 Peripheral Features

6.7.1 Universal Interface Unit

1) UART mode

(T_A= -40~85°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Condition		Specification value Min	Specification value Max	Unit
Transfer rate	2.0V ≤ EV_{DD} ≤ 5.5V	-	-	F_{MCK}/6	bps
		The theoretical value of the maximum transfer rate is F_{MCK}=F_{CLK}	-	10.6	Mbps

(T_A=85~125°C, 2.0V≤EV_{DD}=V_{DD}≤5.5V, V_{SS}=EV_{SS}=0V)

Item	Condition		Specification value Min	Specification value Max	Unit
Transfer rate	2.0V ≤ EV_{DD} ≤ 5.5V	-	-	F_{MCK}/12	bps
		The theoretical value of the maximum transfer rate is F_{MCK}=F_{CLK}	-	5.3	Mbps

Remark: It is guaranteed by the design and not tested in mass production.

2) Three-wire SPI mode (master mode, internal clock output).

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤ 5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85°C		85~125°C		Unit
				Min	Max	Min	Max	
SCLKp cycle time	T_{KCY1}	T_{KCY1} ≥ 2/F_{CLK}	4.0V ≤ EV_{DD} ≤ 5.5V	31.25	-	62.5	-	ns
			2.7V ≤ EV_{DD} ≤ 5.5V	41.67	-	83.33	-	ns
			2.4V ≤ EV_{DD} ≤ 5.5V	65	-	125	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	125	-	250	-	ns
SCLKp high/low level width	T_{KH1},T_{KL1}	4.0V ≤ EV_{DD} ≤ 5.5V		T_{KCY1}/2-4	-	T_{KCY1}/2-7	-	ns
		2.7V ≤ EV_{DD} ≤ 5.5V		T_{KCY1}/2-5	-	T_{KCY1}/2-10	-	ns
		2.4V ≤ EV_{DD} ≤ 5.5V		T_{KCY1}/2-10	-	T_{KCY1}/2-20	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V		T_{KCY1}/2-19	-	T_{KCY1}/2-38	-	ns
SDIp preparation time (to SCLKp↑).	T_{SIK1}	4.0V ≤ EV_{DD} ≤ 5.5V		12	-	23	-	ns
		2.7V ≤ EV_{DD} ≤ 5.5V		17	-	33	-	ns
		2.4V ≤ EV_{DD} ≤ 5.5V		20	-	38	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V		28	-	55	-	ns
SDIp hold time (to SCLKp↑).	T_{KSI1}	2.0V ≤ EV_{DD}≤ 5.5V		5	-	10	-	ns
SCLKp↓→ SDOp output delay time	T_{KSO1}	2.0V ≤ EV_{DD}≤ 5.5V C=20pF Note1		-	5	-	10	ns

Note1: C is the load capacitance of the SCLKp, SDOp output line.

Note: The SDIp pin is selected as the usual input buffer and the SDOp pin and SCLKp pin are selected as the usual output mode through the port input mode register and the port output mode register.

Remark: It is guaranteed by the design and not tested in mass production.

3) Three-wire SPI mode (slave mode, external clock input).

(T_A= -40~125˚C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85°C		85~125˚C		Unit
				Min	Max	Min	Max	
SCLKp cycle time	T_{KCY2}	4.0V ≤ EV_{DD} ≤ 5.5V	20MHz<F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤20MHz	6/F_{MCK}		12/F_{MCK}	-	ns
		2.7V ≤ EV_{DD} ≤ 5.5V	16MHz<F_{MCK}	8/F_{MCK}	-	16/F_{MCK}	-	ns
			F_{MCK}≤16MHz	6/F_{MCK}	-	12/F_{MCK}	-	ns
		2.4V ≤ EV_{DD} ≤ 5.5V		6/F_{MCK} and ≥500	-	12/F_{MCK} and ≥1000	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V		6/F_{MCK} and ≥750	-	12/F_{MCK} and ≥1500	-	ns
SCLKp high/low level width	T_{KH2} T_{KL2}	4.0V ≤ EV_{DD} ≤ 5.5V		T_{KCY1}/2-7	-	T_{KCY1}/2-14	-	ns
		2.7V ≤ EV_{DD} ≤ 5.5V		T_{KCY1}/2-8	-	T_{KCY1}/2-16	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V		T_{KCY1}/2-18	-	T_{KCY1}/2-36	-	ns
SDIp preparation time (to SCLKp↑).	T_{SIK2}	2.7V ≤ EV_{DD} ≤ 5.5V		1/F_{MCK}+20	-	1/F_{MCK}+40	--	ns
		2.0V ≤ EV_{DD} ≤ 5.5V		1/F_{MCK}+30	-	1/F_{MCK}+60		ns
SDIp hold time (to SCLKp↑).	T_{KSI2}	2.0V ≤ EV_{DD} ≤ 5.5V		1/F_{MCK}+31	-	1/F_{MCK}+62	-	ns
SCLKp↓ → SDOp output delay time	T_{KSO2}	2.7V ≤ EV_{DD} ≤ 5.5V C=30pF Note1		-	2/F_{MCK}+ 44	-	2/F_{MCK}+ 66	ns
		2.4V ≤ EV_{DD} ≤ 5.5V C=30pF Note1		-	2/F_{MCK}+ 75	-	2/F_{MCK}+ 113	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C=30pF Note1		-	2/F_{MCK}+ 100	-	2/F_{MCK}+ 150	ns

Note1: C is the load capacitance of the SCLKp and SDOp output lines.

Note: The SDIp pin and SCLKp pin are selected as the usual input buffers and the SDOp pin is selected as the usual output mode through the port input mode register and the port output mode register.

Remark: It is guaranteed by the design and not tested in mass production.

4) Four-wire SPI mode (slave mode, external clock input).

(T_A= -40~125˚C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		-40~85˚C		85~125˚C		Unit
				Min	Max	Min	Max	
SSI00 settling time	T_{SSIK}	DAPmn=0	2.7V ≤ EV_{DD} ≤ 5.5V	120	-	240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	200	-	400	-	ns
		DAPmn=1	2.7V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
SSI00 hold time	T_{KSSI}	DAPmn=0	2.7V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400	-	ns
		DAPmn=1	2.7V ≤ EV_{DD} ≤ 5.5V	120	-	240	-	ns
			2.0V ≤ EV_{DD} ≤ 5.5V	200	-	400	-	ns

Note: The SDIp pin and SCLKp pin are selected as the usual input buffers and the SDOp pin is selected as the usual output mode through the port input mode register and the port output mode register.

Remark: It is guaranteed by the design and not tested in mass production.

5) Simple IIC mode

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	-40~85°C		85~125°C		Unit
			Min	Max	Min	Max	
SCLr clock frequency	F_{SCL}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	-	1000 Note1	-	400 Note1	kHz
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	400 Note1	-	100 Note1	kHz
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5KΩ	-	300 Note1	-	75 Note1	kHz
When SCLr is low hold time	T_{LOW}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	475	-	1200	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	1150	-	4600	-	ns
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5 KΩ	1550	-	6500	-	ns
When SCLr is high hold time	T_{HIGH}	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7 KΩ	475	-	1200	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3 KΩ	1150	-	4600	-	ns
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5KΩ	1550	-	6500	-	ns
Data settling time (received)	$T_{SU:DAT}$	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	1/F_{MCK}+85 Note2	-	1/F_{MCK}+220 Note2	-	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	1/F_{MCK}+145 Note2	-	1/F_{MCK}+580 Note2	-	ns
		2.0V ≤ EV_{DD}≤ 2.7V C_b = 100 pF, R_b = 5KΩ	1/F_{MCK}+230 Note2	-	1/F_{MCK}+1200 Note2	-	ns
Data Hold Time (Send)	$T_{HD:DAT}$	2.7V ≤ EV_{DD} ≤ 5.5V C_b = 50 pF, R_b = 2.7KΩ	-	305	-	770	ns
		2.0V ≤ EV_{DD} ≤ 5.5V C_b = 100 pF, R_b = 3KΩ	-	355	-	1420	ns
		2.0V ≤ EV_{DD} ≤ 2.7V C_b = 100 pF, R_b = 5KΩ	-	405	-	2070	ns

Note1: Must be set to at least F_{MCK}/4.

Note2: The setpoint of F_{MCK} cannot exceed the hold time of SCLr="L" and SCLr="H".

Remark: It is guaranteed by the design and not tested in mass production.

6.7.2 Serial Interface IICA

1) I^2C standard mode

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz	-	100	kHz
The time at which the startup condition was established	$T_{SU:STA}$	-	4.7	-	us
Hold time of the startup condition Note1	$T_{HD:STA}$	-	4.0	-	us
When SCLAr is low, hold time	T_{LOW}	-	4.7	-	us
When SCLAr is high, the hold time is high	T_{HIGH}	-	4.0	-	us
Data settling time (received)	$T_{SU:DAT}$	-	250	-	ns
Data Hold Time (Send) Note2	$T_{HD:DAT}$	-	0	3.45	us
The time at which the stop condition was established	$T_{SU:STO}$	-	4.0	-	us
Bus idle time	T_{BUF}	-	4.7	-	us

Note1: Generates the first clock pulse after the start condition or restart condition is generated.

Note2: The maximum value of $T_{HD:DAT}$ (MAX.) needs to be guaranteed during normal transmission, and it is necessary to wait when performing a reply (ACK).

Note: The values of C_b (communication line capacitance) for each mode and R_b (pull-up resistance value of communication line) at this time are as follows:

Standard mode: C_b=400pF, R_b=2.7kΩ

Remark: It is guaranteed by the design and not tested in mass production.

2) I^2C fast mode

(T_A= -40~125℃,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Quick Mode: F_{CLK}≥3.5MHz	-	400	KHz
The time at which the startup condition was established	$T_{SU:STA}$	-	0.6	-	us
Hold time of the startup condition Note1	$T_{HD:STA}$	-	0.6	-	us
When SCLAr is low, hold time	T_{LOW}	-	1.3	-	us
When SCLAr is high, the hold time is high	T_{HIGH}	-	0.6	-	us
Data settling time (received)	$T_{SU:DAT}$	-	100	-	ns
Data Hold Time (Send) Note2	$T_{HD:DAT}$	-	0	0.9	us
The time at which the stop condition was established	$T_{SU:STO}$	-	0.6	-	us
Bus idle time	T_{BUF}	-	1.3	-	us

Note1: Generates the first clock pulse after the start condition or restart condition is generated.

Note2: The maximum value of $T_{HD:DAT}$ (MAX.) needs to be guaranteed during normal transmission, and it is necessary to wait when performing a reply (ACK).

Note: The values of C_b (communication line capacitance) for each mode and R_b (pull-up resistance value of communication line) at this time are as follows:

Fast mode: C_b=320pF, R_b=1.1kΩ

Remark: It is guaranteed by the design and not tested in mass production.

3) I²C Enhanced Quick Mode

(T_A= -40~125˚C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min	Max	
SCLAr clock frequency	F_{SCL}	Enhanced Quick Mode: F_{CLK}≥10MHz	-	1000	KHz
The time at which the startup condition was established	$T_{SU:\ STA}$	-	0.26	-	us
Hold time of the startup condition Note1	$T_{HD:\ STA}$	-	0.26	-	us
When SCLAr is low, hold time	T_{LOW}	-	0.5	-	us
When SCLAr is high, the hold time is high	T_{HIGH}	-	0.26	-	us
Data settling time (received)	$T_{SU:\ DAT}$	-	50	-	ns
Data Hold Time (Send) Note2	$T_{HD:\ DAT}$	-	0	0.45	us
The time at which the stop condition was established	$T_{SU:\ STO}$	-	0.26	-	us
Bus idle time	T_{BUF}	-	0.5	-	us

Note1: Generates the first clock pulse after the start condition or restart condition is generated.

Note2: It is necessary to guarantee tHD: The maximum value of DAT (MAX.) during normal transmission, and it is necessary to wait when performing a reply (ACK).

Note: The values of C_b (communication line capacitance) for each mode and R_b (pull-up resistance value of communication line) at this time are as follows:

Enhanced Quick Mode: C_b=120pF, R_b=1.1kΩ

Remark: It is guaranteed by the design and not tested in mass production.

6.8 Analog Characteristics

6.8.1 A/D Converter Features

Differentiation of A/D converter characteristics

Reference voltage / Input channel	Reference voltage(+)=AV_{REFP} Reference voltage(-)=AV_{REFM}	Reference voltage(+)=V_{DD} Reference voltage(-)=V_{SS}
ANI0~ ANI15	Refer to 6.8.1(1).	Refer to 6.8.1 (2).
The internal reference voltage, the output voltage of the temperature sensor		

(1) Select the case for reference voltage(+)=AV_{REFP} /ANI0 and reference voltage(-)=AV_{REFM} /ANI1

(T_A= -40~125°C,2.0V≤AV_{REFP}≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=0V,Reference voltage(+)=AV_{REFP}, Reference voltage(-)=AV_{REFM}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	3	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1	-	1	LSB
Differential linearity error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP}≤ 5.5V	-1.5	-	1.5	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion objects: ANI2~ ANI15	2.0V ≤V_{DD}≤ 5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion objects: internal reference voltage, temperature sensor output voltage, PGA output voltage	2.0V ≤V_{DD}≤ 5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} < (Ts / (F_{ADC} x C_{ADC} x ln(2^{12+2})) - R_{ADC})		-	7.5 Note4	-	KΩ
Sampling switch resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitor	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI2~ ANI15		0	-	AV_{REFP}	V
		Internal reference voltage (2.0V≤V_{DD}≤5.5V)		V_{BGR} Note2			V
		The output voltage of the temperature sensor (2.0V≤V_{DD}≤5.5V)		V_{TMPS25} Note2			V

Note1: Does not contain quantization errors (± 1/2 LSB).

Note2: Please refer to " 6.8.2 Characteristics of Temperature Sensors/Internal Reference Voltages".

Note3: F_{ADC} is the operating frequency of AD, and the maximum operating frequency is 48MHz.

Note4: Guaranteed by design, mass production is not tested. The typical value is the default sampling period Ts=13.5, and the conversion speed is the calculated value at F_{ADC}=48MHz.

(2) Select the case of reference voltage (+) =V_{DD} and reference voltage (-) =V_{SS}

(T_A= -40~125℃, 2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V,Reference Voltage(+)=V_{DD}, Reference Voltage (-) =V_{SS})

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-		-	12	-	bit
Combined error Note1	ET	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-	-	-	LSB
Zero scale error Note1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-	-	-	LSB
Full scale error Note1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-	-	-	LSB
Integral linearity error Note1	EL	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-2	-	2	LSB
Differential linearity error Note1	ED	12-bit resolution	2.0V ≤AV_{REFP}≤5.5V	-3	-	3	LSB
Conversion time Note3	T_{CONV}	12-bit resolution Conversion objects:	2.0V≤V_{DD}≤5.5V	45	-	-	1/fadc
		12-bit resolution Conversion objects: internal reference voltage, output voltage of	2.0V≤V_{DD}≤5.5V	72	-	-	1/fadc
External input resistance	R_{AIN}	R_{AIN} < (Ts / (F_{ADC} x C_{ADC} x ln(2^{12+2})) - R_{ADC})			7.5 Note4	-	kΩ
Sampling switch resistance	R_{ADC}	-		-		1.5	kΩ
Sample-and-hold capacitor	C_{ADC}	-		-	2		pF
Analog input voltage	V_{AIN}	ANI0~ ANI7		0		V_{DD}	V
		ANI8~ ANI15		0		EV_{DD}	V
		Internal reference voltage (2.0V≤V_{DD}≤5.5V)		V_{BGR} Note2			V
		The output voltage of the temperature sensor (2.0V≤V_{DD}≤5.5V)		V_{TMPS25} Note2			V

Note1: Does not contain quantization errors (± 1/2 LSB).

Note2: Please refer to " 6.8.2 Characteristics of Temperature Sensors/Internal Reference Voltages".

Note3: F_{ADC} is the operating frequency of AD, and the maximum operating frequency is 48MHz.

Note4: Guaranteed by design, mass production is not tested. The typical value is the default sampling period Ts=13.5, and the conversion speed is F_{ADC}=64MHz.

6.8.2 Characteristics of The Temperature Densor/Internal Reference Voltage

(T_A= -40~125°C,2.0V≤V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
The output voltage of the temperature sensor	V_{TMPS25}	T_A=25°C	-	1.09	-	V
Internal reference voltage	V_{BGR}	T_A= -40~10°C	1.25	1.45	1.65	V
		T_A=10~70°C	1.38	1.45	1.50	V
		T_A=70~125°C	1.35	1.45	1.55	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/°C
Run stable wait time	T_{AMP}	-	5	-	-	ms

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.8.3 D/A Converter

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
resolution	RES	-	-	-	-	8	bit
Combined error	ET	Rload=4MΩ	2.0V≤V_{DD}≤5.5V	-2.5	-	2.5	LSB
Stabilization time	T_{SET}	Cload=20pF	2.7V≤V_{DD}≤5.5V	-	-	3	ms
			2.0V≤V_{DD}<2.7V	-	-	6	ms
Output impedance	RO	Rload=4MΩ	2.0V≤V_{DD}≤5.5V	4.7	-	8	KΩ

Remark: Low temperature specification value is guaranteed by the design, and low temperature conditions are not measured in mass production.

6.8.4 Comparator

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Input deviation voltage	V_{OFFSET}	-		-	±10	±40	mV
Input voltage range	V_{IN}	-		0	-	V_{DD}	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register: 7FH ~ 80H (m = 0, 1).		-	-	±2	LSB
		other		-	-	±1	LSB
Response time	T_{CR}, T_{CF}	The input amplitude ± 100mV		-	70	125	ns
Run settling time Note1	T_{STB}	CMPn=0->1	V_{DD}= 3.3 ~ 5.5V	-	-	1	ms
			V_{DD}= 2.0 ~ 3.3V	-	-	3	
Reference settling time	T_{VR}	CVRE=0->1 Note2		-	-	20	ms
Operating current	I_{CMPDD}	Refer to 6.5.2 Supply current characteristics					-

Note 1: The time required from comparator action enable (CMPnEN=0->1) to meeting the various DC/AC style requirements of the CMP.

Note2: By setting the CVREm bit to 1; m = 0 to 1), the reference settling time is passed before the comparator output can be enabled (CnOE bit = 1; n = 0 to 1)

Remark: It is guaranteed by the design and not tested in mass production.

6.8.5 Programmable Gain Amplifier PGA

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input deviation voltage	V_{IOPGA}	-		-	-	±10	mV
Input voltage range	V_{IPGA}	-		0	-	0.9xV_{DD}/Gain	V
Output voltage range	V_{IOHPGA}	-		0.93xV_{DD}	-	-	V
	V_{IOLPGA}	-		-	-	0.07xV_{DD}	V
Gain deviation		x4	-	-	-	±1	%
		x8	-	-	-	±1	%
		x10	-	-	-	±1	%
		x12	-	-	-	±2	%
		x14	-	-	-	±2	%
		x16	-	-	-	±2	%
		x32	-	-	-	±3	%
Conversion rate	SR_{RPGA}	Rising Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5V (other than x32)	3.5	-	-	V/us
			4.0 V ≤ V_{DD} ≤ 5.5V (x32)	3.0	-	-	
			2.0 V ≤ V_{DD} ≤ 4.0V	0.5	-	-	
	SR_{FPGA}	Falling Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0V ≤ V_{DD} ≤ 5.5V (other than x32)	3.5	-	-	
			4.0V ≤ V_{DD} ≤ 5.5V (x32)	3.0	-	-	
			2.0V ≤ V_{DD} ≤ 4.0V	0.5	-	-	
Run settling time Note1	T_{PGA}	x4	-	-	-	5	us
		x8	-	-	-	5	us
		x10	-	-	-	5	us
		x12	-	-	-	10	us
		x14	-	-	-	10	us
		x16	-	-	-	10	us
		x32	-	-	-	10	us
Operating current	I_{PGADD}	Refer to 6.5.2 Supply current characteristics					

Note1: The time required from PGA action enable (PGAEN=1) to meeting the various DC and AC style requirements of the PGA.

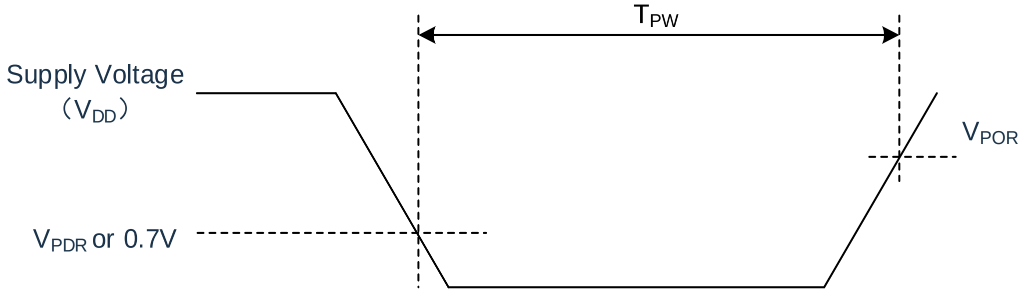
Note2: It is guaranteed by the design and not tested in mass production.

6.8.6 POR Circuit Characteristics

(T_A= -40~125°C,V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{POR}	When the supply voltage rises	-	1.60	2.0	V
	V_{PDR}	When the supply voltage drops	1.37	1.50	-	V
Minimum pulse width Note1	T_{PW}	-	300	-	-	μs

Note1: This is the time required for the POR to reset when V_{DD} is lower than V_{PDR}. In addition, in deep sleep mode, the bit0 (HIOSTOP) and bit7(MSTOP) stops the oscillation of the main system clock (F_{MAIN}) from V_{DD} below 0.7V to a rebound above V_{POR} The time required for reset up to POL.



Remark: It is guaranteed by the design and not tested in mass production.

6.8.7 LVD Circuit Characteristics

(1) Reset mode and interrupt mode

(T_A= -40~125°C,V_{PDR}≤V_{DD}≤5.5V,V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection voltage	V_{LVD0}	When the supply voltage rises	-	4.06	4.26	V
		When the supply voltage drops	3.78	3.98	-	V
	V_{LVD1}	When the supply voltage rises	-	3.75	-	V
		When the supply voltage drops	-	3.67	-	V
	V_{LVD2}	When the supply voltage rises	-	3.02	-	V
		When the supply voltage drops	-	2.96	-	V
	V_{LVD3}	When the supply voltage rises	-	2.71	-	V
		When the supply voltage drops	-	2.65	-	V
	V_{LVD4}	When the supply voltage rises	-	2.09	2.16	V
		When the supply voltage drops	1.97	2.04	-	V
Minimum pulse width	T_{LW}	-	300	-	-	μs
Detection delay	-	-		-	300	μs

Remark: It is guaranteed by the design and not tested in mass production.

(2) Interrupt & reset mode

(T_A= -40~125°C,V_{PDR} ≤V_{DD}≤5.5V,V_{SS}=0V)

Item	Symbol	Condition			Min	Typ	Max	Unit
Interrupt & reset mode	V_{LVDB0}	V_{POC2}=0	drop reset voltage		1.78	1.84	-	V
	V_{LVDB2}	V_{POC1}=0	LVIS1=0	Rise reset release voltage	-	2.09	2.16	V
		V_{POC0}=1	LVIS0=1	Drop the interrupt voltage	1.97	2.04	-	V
	V_{LVDC0}		drop reset voltage		-	2.45	-	V
	V_{LVDC2}	V_{POC2}=0	LVIS1=0	Rise reset release voltage	-	2.71	-	V
		V_{POC1}=1	LVIS0=1	Drop the interrupt voltage	-	2.65	-	V
	V_{LVDC3}	V_{POC0}=0	LVIS1=0	Rise reset release voltage	-	3.75	-	V
			LVIS0=0	Drop the interrupt voltage	-	3.67	-	V
	V_{LVDD0}		down reset voltage		-	2.75	-	V
	V_{LVDD2}	V_{POC2}=0	LVIS1=0	Rise reset release voltage	-	3.02	-	V
		V_{POC1}=1	LVIS0=1	Drop the interrupt voltage	-	2.96	-	V
	V_{LVDD3}	V_{POC0}=1	LVIS1=0	Rise reset release voltage	-	4.06	4.26	V
			LVIS0=0	Drop the interrupt voltage	3.78	3.98	-	V

Remark: It is guaranteed by the design and not tested in mass production.

6.8.8 Reset Time Versus Rising Slope Characteristics of The Supply Voltage

(T_A= -40~125℃,V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Reset time	T_{RESET}	-	-	1	-	ms
The rising slope of the supply voltage	S_{VDD}	-	-	-	54	V/ms

Remark: It is guaranteed by the design and not tested in mass production.

6.9 Memory Feature

6.9.1 Flash Memory Feature

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Conditions	Min	Max	Unit
Tprog	Word Program(32bit)	T_A= -40~125°C	24	30	μs
Terraces	Sector erase	T_A= -40~125°C	4	5	ms
	Chip erase	T_A= -40~125°C	20	40	ms
N_{END}	Endurance	T_A= -40~125°C	100	-	kcycle
T_{RET}	Data retention	100 kcycle [Note1] at T_A=125°C	20	-	Years

Note1: Cycling performed over the whole temperature range.

Remark: It is guaranteed by the design and not tested in mass production.

6.9.2 RAM Memory Feature

(T_A= -40~125°C,2.0V≤EV_{DD}=V_{DD}≤5.5V,V_{SS}=EV_{SS}=0V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{RAMHOLD}$	RAM Hold Voltage	T_A= -40~125°C	0.8	-	V

Remark: It is guaranteed by the design and not tested in mass production.

6.10 Electrical Sensitivity Characteristics

6.10.1 Electrostatic Discharge (ESD) Feature

Symbol	Parameter	Conditions	Class
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25°C JEDEC EIA/JESD22- A114	3A

Remark: It is guaranteed by the design and not tested in mass production.

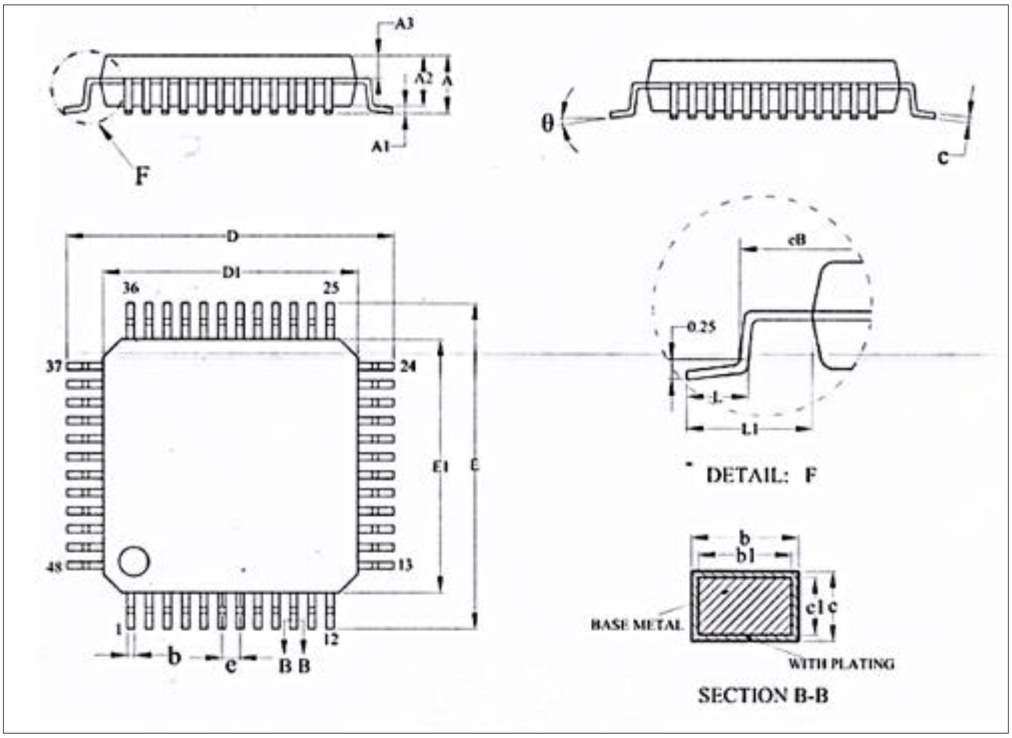
6.10.2 Static Latch-up (LU) Feature

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	JEDEC STANDARD NO.78E NOVEMBER 2016	Class ⅡA (T_A=125°C)

Remark: It is guaranteed by the design and not tested in mass production.

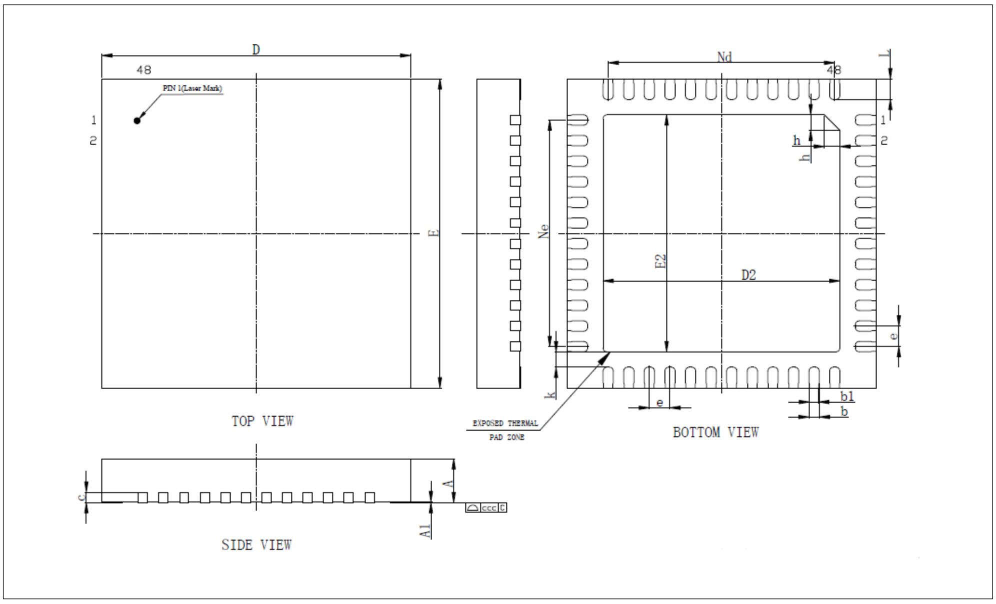
7 Package Information

7.1 LQFP48(7x7mm, 0.5mm)



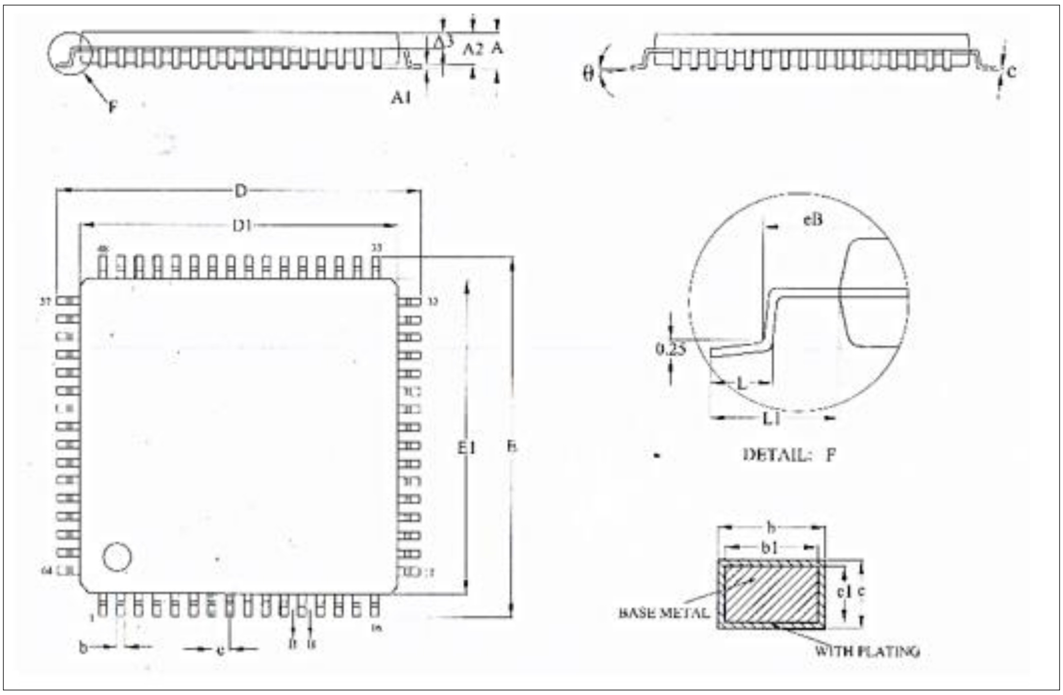
Symbol	Millimetre		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.2 QFN48(6x6, 0.4mm)



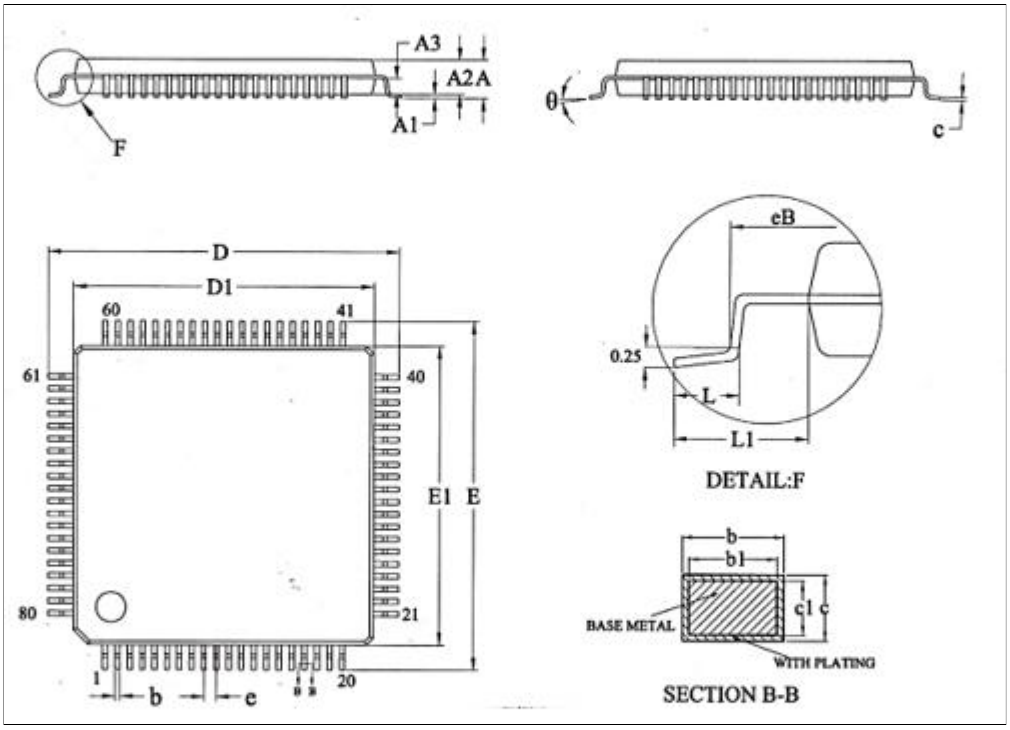
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.18REF		
c	0.203REF		
D	5.90	6.00	6.10
D2	4.55	4.60	4.65
e	0.40BSC		
Nd	4.40BSC		
Ne	4.40BSC		
E	5.90	6.00	6.10
E2	4.55	4.60	4.65
L	0.35	0.40	0.45
h	0.25	0.30	0.35
R	0.075REF		
k	0.25	0.30	0.35
ccc	0.08		

7.3 LQFP64(7x7, 0.4mm)



Symbol	Millimetre		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.4 LQFP80(12x12, 0.5mm)



Symbol	Millimetre		
	Min	Name	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
eB	13.05	-	13.25
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	-	7°

8 Revision History

Revision	Date	Modify content
V1.00	Aug 2022	Internal First Edition
V1.01	Nov 2022	Modified the parameters in 6.5.1
V1.0.2	Feb 2023	1) Supplement the standard grade of automobile products in chapter 1.1 2) Supplement the remarks of parameters at low temperature 3) Correct the product pin function description in section 4.1 4) Optimize format 5) 6.5.2 Supply Current Characteristics correct maximum parameter
V1.0.3	Mar 2023	1) 1.3.4, 4.1.3 P137 Pin function SI00 corrected to SDI00 2) Corrected 7.4 package Information
V1.0.4	May 2023	Update 7.2 package Information